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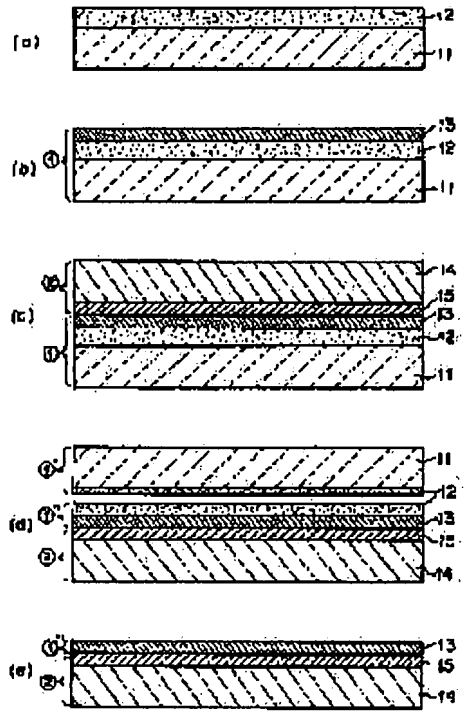
(54) MANUFACTURE OF SEMICONDUCTOR SUBSTRATE

(57)Abstract:

PURPOSE: To remarkably lessen the defects in the single crystalline layer on an insulator by sticking a second substrate onto the nonporous single crystalline semiconductor layer made on the porous layer of a first substrate, and then, separating these two substrate at the porous layer, and then, removing the second substrate and the porous layer on the first substrate.

CONSTITUTION: The surface layer of an Si single crystalline substrate 11 is made porous 12, and a nonporous single crystalline Si layer 13 is made hereon. Next, another Si supporting substrate 14 and the single crystalline Si layer 13 are stuck fast to each other through an insulating layer 15 at high temperature, and then those are stuck together by anode junction, pressurization, or heat treatment, or these combination. Next, the boards are separated at the porous Si layer 12. Furthermore, the porous Si layer 12 is removed selectively. That is, the



single crystallized Si layer 13 in film shape is left on the insulating substrate 15+14 by etching only the porous Si layer 12 by electroless wet chemical etching. Alternatively, with the single crystalline Si layer 13 as a polishing stopper, the porous Si layer 12 is removed by selective polishing.

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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The process which forms a nonvesicular single crystal half conductor layer on said porous layer of the 1st base which has a porous layer, The process which sticks said nonvesicular single crystal half conductor layer with the 2nd base, the process which sticks and separates said constituted base in said porous layer, The production approach of the semi-conductor substrate characterized by having the process which removes the porous layer allotted on said 2nd separated base, and the process which removes the porous layer which constitutes said 1st separated base.
[Claim 2] The process which forms a nonvesicular single crystal half conductor layer on said porous layer of the 1st base which has a porous layer, The process which sticks said nonvesicular single crystal half conductor layer through the 2nd base and insulating layer, The production approach of the semi-conductor substrate characterized by having the process which sticks and separates said constituted base in said porous layer, the process which removes the porous layer allotted on said 2nd separated base, and the process which removes the porous layer which constitutes said 1st separated base.
[Claim 3] Said porous layer is the production approach of claim 1 constituted using silicon, or a semi-conductor substrate according to claim 2.
[Claim 4] The production approach of claim 1 which performs the process after said lamination process as the 1st base which newly forms a porous layer in the base which removes the porous layer which constitutes said 1st separated base, and is obtained, and has said porous layer for this in it, or a semi-conductor substrate according to claim 2.
[Claim 5] Said nonvesicular single crystal half conductor layer is the production approach of claim 1 which is Si layer, or a semi-conductor substrate given in 2.
[Claim 6] Said nonvesicular single crystal half conductor layer is the production approach of claim 1 which is a compound semiconductor layer, or a semi-conductor substrate given in 2.
[Claim 7] Said 1st base is the production approach of claim 1 constituted using Si, or a semi-conductor substrate given in 2.
[Claim 8] Said 2nd base is the production approach of claim 1 which is a light transmission nature base, or a semi-conductor substrate given in 2.
[Claim 9] Removal of said porous layer is the production approach of claim 1 made using etching, or a semi-conductor substrate given in 2.
[Claim 10] Removal of said porous layer is the production approach of claim 1 made by grinding alternatively said nonvesicular single crystal half conductor layer for said porous layer as a stopper, or a semi-conductor substrate given in 2.
[Claim 11] The separation in said porous layer is the production approach of claim 1 performed by at least one or more approaches of pressurizing in the perpendicular direction to the lamination side of the stuck base, pulling in the direction perpendicular to said field, and applying-to this lamination side-shearing stress **, or a semi-conductor substrate given in 2.
[Claim 12] Said insulating layer is the production approach of the semi-conductor substrate according to claim 2 formed at least in one side on the front face of said 2nd base on said nonvesicular single crystal

layer.
[Claim 13] Said insulating layer is the thermal oxidation film and deposition SiO2. The film and deposition Si3 N4 The production approach of the semi-conductor substrate according to claim 12 chosen from film.
[Claim 14] Said lamination process is the production approach of the semi-conductor substrate according to claim 1 or 2 performed by anode plate junction, pressurization, heat treatment, or the approach chosen from such combination.
[Claim 15] Said porous layer is the production approach of the semi-conductor substrate according to claim 1 or 2 formed using anodization.
[Claim 16] Said anodization is the production approach of the semi-conductor substrate according to claim 15 performed in HF solution.
[Claim 17] The separation in said porous layer is the production approach of claim 1 performed by impressing wave energy to this porous layer, or a semi-conductor substrate given in 2.
[Claim 18] The separation in said porous layer is the production approach of claim 1 performed by inserting the member for exfoliation from this porous layer side face, or a semi-conductor substrate given in 2.
[Claim 19] The separation in said porous layer is the production approach of claim 1 performed by the expansion energy of the matter into which this porous layer was infiltrated, or a semi-conductor substrate given in 2.
[Claim 20] The separation in said porous layer is the production approach of claim 1 performed by the selective etching to this porous layer of a wafer side face, or a semi-conductor substrate given in 2.
[Claim 21] The porosity of said porous layer is the production approach of claim 1 in 10 - 80% of range, or a semi-conductor substrate given in 2.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the production approach of a semi-conductor substrate. Furthermore, it is related with the production approach of the production approach of dielectric separation or the single crystal semiconductor of an insulating lifter, and the single crystal compound semiconductor on a half-dynamic body substrate, the electron device further created by the single crystal half conductor layer, and the semi-conductor substrate suitable for an integrated circuit in detail.
[0002]
[Description of the Prior Art] Formation of the single crystal Si semi-conductor layer of an insulating lifter is silicon. ON It was widely known as an insulator (SOI) technique, and in the bulk Si substrate which produces the usual Si integrated circuit, since the device using a SOI technique has many dominance points which cannot reach, many researches have accomplished. That is, the possibility of the perfect depletion mold field-effect transistor by the formation of 6. thin film which can prevent 5. latch rise which 3. stray capacity 1. dielectric separation excels [stray capacity] in the possibility of high integration and 2. opposite radiation resistance easily is reduced, and can skip the possibility of improvement in the speed and 4. well process by using a SOI technique, and the dominance point of ** are acquired.
[0003] In order to realize many advantages on a device property which was described above, it has inquired about the formation approach of SOI structure over the past dozens of years. These contents are summarized in the following reference.
[0004] Special Issue:"Single-crystal silicon on non-single-crystal insulators";edited by G.W.Cullen and Journal of Crystal Growth and volume 63, no3, and pp429-590(1983). -- in ancient times again SOS (silicon ON sapphire) which is made to carry out hetero epitaxy of the Si, and forms it by CVD (chemistry gaseous-phase method) on single crystal silicon on sapphire is known, and a success temporary as a SOI technique which matured most is stored. A fraction The breadth of the application is barred by the grid mismatching of Si layer and a substrate silicon-on-sapphire interface by the expensive rank of a substrate, and the delay to large-area-izing rather than mixing to a lot of crystal defects and Si layer of the aluminum from silicon on sapphire, and anything. The attempt in which SOI structure will be realized without using silicon on sapphire is performed comparatively at recent years. This attempt is divided roughly into the following two.
[0005] 1. Open an aperture for Si single crystal substrate after scaling, make Si substrate express partially, carry out epitaxial growth to a longitudinal direction by considering the part as seed, and it is SiO2. Si single crystal layer is formed upwards. (In this case, SiO2. It is accompanied by deposition of Si layer upwards)
2. Use the Si single crystal substrate itself as a barrier layer, and it is SiO2 to the lower part. It forms. (This approach is not accompanied by deposition of Si layer.) The device on a compound semiconductor has the high engine performance which is not obtained, for example, a high speed, luminescence, etc. by Si again. Most of these devices carries out epitaxial growth on compound semiconductor substrates,

such as GaAs, and current is made in it.
[0006] However, a compound semiconductor substrate is expensive, a mechanical strength is low, and a large area wafer has which trouble with difficult creation.
[0007] From such a thing, it is cheap, and a mechanical strength is also high and the attempt which carries out heteroepitaxial growth of the compound semiconductor on Si wafer which can produce a large area wafer is made.
[0008]
[Problem(s) to be Solved by the Invention] As a means to realize the above 1, the approach and amorphous Si to which longitudinal direction epitaxial growth of the single crystal layer Si is carried out are directly deposited by CVD. The approach, amorphous substance which carry out solid phase longitudinal direction epitaxial growth by heat treatment or a polycrystal Si layer -- energy beams, such as an electron ray and laser light, -- converging -- irradiating -- melting recrystallization -- a single crystal layer -- SiO2 the approach of making it growing up upwards -- and The approach (Zone Melting Recrystallization) of scanning a melting field to band-like at a cylindrical heater is learned. Although there are merits and demerits in these approaches, respectively, it has left the great problem to the controllability, productivity, homogeneity, and quality, and there is nothing that was still put in practical use industrially. For example, in order to form a flat thin film, sacrifice oxidation is needed and the crystallinity of a CVD method is bad in a solid phase grown method. Moreover, by the beam annealing method, a problem is in the processing time by convergence beam scan, and controllabilities, such as lap condition of a beam, and focus control. Among these, Zone Melting Although the Recrystallization method has matured most and the comparatively large-scale integrated circuit is also made as an experiment, remaining and creating a minority carrier device does not still have many crystal defects, such as a subgrain boundary, very much.
[0009] In the approach of not using Si substrate which is the approach of the above 2 as a seed of epitaxial growth, four kinds of approaches as follows are mentioned.
[0010] 1. Form an oxide film in Si single crystal substrate with which anisotropic etching of the slot on the V type was carried out to the front face, and form Si single crystal field as for which was surrounded by the V groove and dielectric separation was carried out by polish on the thick polycrystal Si layer from the rear face of Si substrate after depositing a polycrystal Si layer thickly on this oxide film degree it is the same as Si substrate. In this technique, although crystallinity is good, a problem is in the process which deposits the hundreds of microns polycrystal Si thickly, and the process which leaves only Si barrier layer which ground the single crystal Si substrate from the rear face, and was separated from the point of a controllability and productivity.
[0011] 2. It is SiO2 by the ion implantation of oxygen in Si single crystal substrate called SIMOX (SIMOX:Seperation by ion implanted oxygen). It is the approach of forming a layer, and since Si process and adjustment are good, they are current but the technique of having matured. However, SiO2 It is oxygen ion in order to form a layer 1018 ions/cm2 Although it is necessary to also pour in the above, the impregnation time amount is huge, it cannot say that productivity is high and wafer cost is high. Furthermore, many crystal defects remain, are seen industrially and it has not resulted in sufficient quality which can produce a minority carrier device.
[0012] 3. How to form SOI structure according to dielectric separation by oxidation of Porosity Si. This approach is the approach of carrying out dielectric separation of the N type Si island by accelerating oxidation, after porosity-izing only a P type Si substrate by the anodization method in HF solution so that an N type Si layer may be formed in a P type Si single crystal substrate front face at island shape by the proton ion implantation, (J.Crystal Growth besides Imai, vol 63,547) (1983), or epitaxial growth and patterning and Si island may be surrounded from a front face. By this approach, Si field separated is determined before the device process, and there is a trouble that the degree of freedom of a device design may be restricted.
[0013] Moreover, apart from the formation approach of the above conventional SOI, the approach of using heat treatment or adhesives for another Si single crystal substrate which oxidized Si single crystal substrate thermally, and forming lamination and SOI structure is capturing the spotlight in recent years.

This approach needs to thin-film-ize the barrier layer for a device to homogeneity. That is, it is necessary to thin-film-ize Si single crystal substrate with a thickness of hundreds of microns less than [micron order or it]. There are two kinds of approaches in this thin film-ization as follows.
[0014] 1. It is difficult to thin-film-ize to homogeneity in polish of the thin-film-izing 1 by the thin film-ized 2. selective etching by polish. Especially as for submicron thin film-ization, dispersion also becomes dozens of% and this equalization poses a big problem. If diameter-ization of macrostomia of a wafer furthermore progresses, whenever [the / difficult] will just increase.
[0015] Moreover, although etching of 2 is confirmed to uniform thin-film-izing - At most 102 - ion implantation with the bad front-face nature after - etching whose selection ratio is not enough, since the epitaxial growth or heteroepitaxial growth on a high concentration B dope Si layer is used, there are troubles, like the crystallinity of a SOI layer is bad (C. -- Harendt, et.al., and J.Elect.Mater.Vol.20,267 (1991) --) H. Baumgart, et.al., Extended Abstract of ECS 1st International Symposium of Wafer Bonding pp-733 (1991), C. E.Hunt, Extended Abstract ofECS 1st International Symposium of Wafer Bonding, pp-696 (1991).
[0016] Furthermore the semi-conductor substrate using lamination surely needs two wafers, and among those, most will almost be vainly removed by polish, etching, etc., and one sheet will be thrown away, and will waste the resource of the limited earth.
[0017] Therefore, in SOI by lamination, many troubles exist in the controllability and a homogeneous pan by the present approach at economical efficiency.
[0018] Moreover, on the light transmission nature substrate represented by glass, generally, from the disorderly nature of the crystal structure, reflecting the disorderly nature of a substrate, the deposited thin film Si layer is not good, and turns into only a polycrystal layer in an amorphous substance, and a highly efficient device cannot be produced. It gets down from it according to the crystal structure of a substrate being amorphous, and even if it deposits Si layer, a good single crystal layer is not only obtained.
[0019] By the way, a light transmission nature substrate constitutes the contact sensor and projection mold liquid crystal image display device which are an optical photo detector, and also is important. and the pixel (picture element) of a sensor or a display -- more -- much more -- densification and high-resolution-izing -- in order to carry out high elaboration, a highly efficient driver element is needed. Consequently, it is necessary to be produced using the single crystal layer which has the crystallinity which was excellent also as a component prepared on the light transmission nature substrate.
[0020] Therefore, it is difficult to produce the crystal structure with many the defect, therefore the driver element which had sufficient engine performance to be required from now on or it was required in amorphous Si or Polycrystal Si.
[0021] As stated in the top, the substrate of a compound semiconductor is indispensable to device production of a compound semiconductor. However, the substrate of a compound semiconductor is expensive and, moreover, large-area-izing is very difficult for it.
[0022] Furthermore, although to carry out epitaxial growth of the compound semiconductors, such as GaAs, on Si substrate is tried, it is very difficult for the growth film to have bad crystallinity and to apply to a device by the difference in a lattice constant or a coefficient of thermal expansion.
[0023] Moreover, although to carry out epitaxial growth of the compound semiconductor on Porosity Si is tried in order to ease the misfit of a grid, the stability as a substrate under production or after producing, and dependability are missing in a device with the lowness of the thermal stability of Porosity Si, aging, etc.
[0024] Meanwhile, Takao Yonehara who is the artificer of this invention proposed the manufacture approach of the new semi-conductor member previously indicated by JP,5-21338,A in view of the technical-problem point mentioned above.
[0025] The approach indicated by the official report concerned is a thing as follows. That is, after it forms the member which allotted the nonvesicular single crystal semiconductor region on a porosity single crystal semiconductor region and a front face sticks the front face of the member which consisted of insulating matter on the front face of said nonvesicular single crystal semiconductor region, it is the

manufacture approach of the semi-conductor member characterized by removing said porosity single crystal semiconductor region by etching.
[0026] The approach concerned can solve the technical problem mentioned above, and is excellent. However, if the approach indicated by the official report concerned is developed further and improvement in the productivity of a semi-conductor substrate and low cost-ization can be attained further, the contribution to the industry concerning the technical field concerned will become very big.
[0027] [Purpose of invention] this invention aims at offering the production approach of a semi-conductor substrate of having improved further the approach indicated by the above-mentioned official report.
[0028] another purpose of this invention -- economical efficiency -- excelling -- a large area -- crossing -- homogeneity -- it leaves the semi-conductor layer or compound semiconductor barrier layer formed in the front face using the flat single crystal substrate which has the extremely excellent crystallinity, this from the one side to barrier layer is removed, and it is in offering the production approach of a semi-conductor substrate of obtaining few remarkable single crystal layers or compound semiconductor crystal layer of a defect to an insulating lifter.
[0029] Still more nearly another purpose of this invention is to propose the production approach of the semi-conductor substrate which stood high in the field of productivity, homogeneity, a controllability, and cost on the transparence substrate (light transmission nature substrate) when crystallinity obtained Si which was excellent just like the single crystal wafer, or a compound semiconductor single crystal layer.

[0030] Also in case still more nearly another purpose of this invention produces the large-scale integrated circuit of SOI structure, it is to propose the production approach of expensive SOS and the alternative ********** substrate of SIMOX.
[0031]
[Means for Solving the Problem] The production approach of the semi-conductor substrate of this invention is the thing of a configuration of lower-**(ing).
[0032] Namely, the 1st mode of the production approach of the semi-conductor substrate of this invention The process which forms a nonvesicular single crystal half conductor layer on said porous layer of the 1st base which has a porous layer, The process which sticks said nonvesicular single crystal half conductor layer with the 2nd base, the process which sticks and separates said constituted base in said porous layer, It is characterized by having the process which removes the porous layer allotted on said 2nd separated base, and the process which removes the porous layer which constitutes said 1st separated base.
[0033] The process which forms a nonvesicular single crystal half conductor layer on said porous layer of the 1st base with which the 2nd mode of this invention has a porous layer, The process which sticks said nonvesicular single crystal half conductor layer through the 2nd base and insulating layer, It is characterized by having the process which sticks and separates said constituted base in said porous layer, the process which removes the porous layer allotted on said 2nd separated base, and the process which removes the porous layer which constitutes said 1st separated base.
[0034]
[Function] In this invention, it sticks, the constituted base is separated by the porous layer, and the semi-conductor base with which the quality nonvesicular single crystal half conductor layer was allotted can be formed by removing the porous layer on the 2nd base to which the nonvesicular single crystal half conductor layer was allotted. In addition, it can stick, the constituted base can be separated by the porous layer, and the 1st base from which the porous layer was removed can be reused to semi-conductor base production by removing the porous layer which constitutes the 1st base. Thereby, improvement in the productivity of a semi-conductor base and low cost-ization can be attained further.
[0035] According to this invention, the production approach of the semi-conductor substrate which stood high in the field of productivity, homogeneity, a controllability, and cost on substrates including a transparence substrate (light transmission nature substrate) when crystallinity obtained a single crystal layer or compound semiconductor single crystal layers, such as Si which was excellent just like the

single crystal wafer, can be proposed.
[0036] Moreover, according to this invention, also in case the large-scale integrated circuit of SOI structure is produced, the production approach of expensive SOS and the alternative ********** substrate of SIMOX can be proposed.
[0037] In this invention, a base is separable into two or more through a porous layer, and after one base after separation removes residual porosity, it is usable as a semi-conductor substrate, and after removing residual porosity, it is applicable [the base of another side] to production of a semi-conductor substrate again.
[0038] In this invention, a porous layer and a nonvesicular single crystal layer are formed in both sides of a base, and after sticking another base of two sheets so that this single crystal layer may be pinched, two semi-conductor substrates are producible to coincidence by separating a base by said porous layer.
[0039] The production approach of the semi-conductor substrate of this invention is mentioned as an example, and silicon is explained below at a detail.
[0040] Although the mechanical strength of Porosity Si changes with porosit(ies), it is thought that it is weaker enough than bulk Si. For example, as long as porosity is 50%, a mechanical strength may consider the one half of bulk. That is, it compresses into a lamination wafer, and when it pulls or shearing force is applied, a porosity Si layer will be destroyed first. Moreover, if porosity is made to increase, a porous layer can be destroyed by the weaker force.
[0041] Si substrate can be made to porosity-ize by the anodization method which used HF solution. This porosity Si layer is consistency 2.33 g/cm3 of a single crystal Si. That consistency can be changed to the range of 1.1 - 0.6 g/cm3 by comparing and changing HF solution concentration to 50 - 20%. This porous layer is not formed in an N type Si layer of the following reason, but is formed only in a P type Si substrate of it. According to observation according [this porosity Si layer] to a transmission electron microscope, the hole of a diameter with an average of about 600A is formed.
[0042] Porosity Si was discovered by Uhlir etc. in the research process of electrolytic polishing of a semi-conductor in 1956 (A. Uhlir, Bell Syst.Tech.J., vol.35,333 (1956)).
[0043] Moreover, Unagami etc. studied the lytic reaction of Si in anodization, an electron hole is required for the anodic reaction of Si in HF solution, and the reaction has reported that it is as follows (T. Unagami, J.Electrochem.Soc., vol.127,476 (1980)).
[0044] Si+2HF+(2-n) e+->SiF2+2H++ne-SiF2+2 HF->SiF4+H2SiF4+2 HF->H2 SiF6 or Si+4HF+(4-lambda) e+->SiF4+4H++lambdae-SiF4+2 HF->H2 SiF6 -- here -- e+ And e- The electron hole and the electron are expressed, respectively. Moreover, n and lambda are the number of electron holes required in order that a Sil atom may dissolve, respectively, and when n> 2 or the conditions which become lambda>4 are fulfilled, they suppose that Porosity Si is formed.
[0045] Although P type Si in which an electron hole exists is porosity-ized from the above thing, N type Si is not porosity-ized. The selectivity in this porosity-izing is proved [Imai /, such as Nagano,] (KImai, Solid-State Electronics, vol.24,159 (1981)). (Nagano, Nakajima, Yasuno, Onaka, Kajiwara, the Institute of Electronics and Communication Engineers technical research report, vol.79, SSD 79-9549 (1979))
[0046] However, it is important to choose the substrate which a report that it is porosity-ized also has if it is high concentration N type Si (R. P.Holmstrom and J.Y.Chi, Appl.Phys.Lett., vol.42,386 (1983)), and is not scrupulous according to P type and N type, and can realize porosity-ization.
[0047] According to observation by the transmission electron microscope, although the hole of a diameter with an average of about 600A is formed and the consistency becomes below one half compared with a single crystal Si, single crystal nature is maintained by the porosity Si layer, and it is also possible in it to carry out epitaxial growth of the single crystal Si layer to the upper part of a porous layer. However, above 1000 degrees C, the rearrangement of an internal hole happens and the property of accelerating etching is spoiled. For this reason, low-temperature growth of molecular-beam epitaxial growth, plasma CVD, a reduced pressure CVD method, Light CVD, a bias sputtering technique, a liquid phase grown method, etc. is made suitable at the epitaxial growth of Si layer.
[0048] Moreover, since a lot of [a porous layer] openings to the interior are formed, a consistency decreases below in one half. Consequently, since surface area increases by leaps and bounds compared

with the volume, compared with the etch rate of the usual single crystal layer, it accelerates the chemical etching rate remarkably.
[0049] As shown in [example 1 of embodiment] drawing 1 (a), 1st Si single crystal substrate 11 is prepared first, the surface layer is carried out porosity-ized 12, and the nonvesicular single crystal Si layer 13 is formed on porosity Si 12 (drawing 1 (b)).
[0050] Next, as shown in drawing 1 (c), after sticking another Si support substrate 14 and single crystal Si layer 13 at a room temperature through an insulating layer 15, it sticks with anode plate junction, pressurization, heat treatments, or such combination. This combines firmly Si support substrate 14 and the single crystal layer 13 through an insulating layer 15. Or it forms an insulating layer 15 at least in one side on a single crystal Si layer and Si support substrate 14, it is stuck by the three-sheet pile on both sides of insulating sheet metal.
[0051] Next, a substrate is separated in the porosity Si layer 12 (drawing 1 (d)). Si support substrate side serves as structure like the 15/Si support substrate 14 of 13/insulating layers of porosity Si12/single crystal Si layers.
[0052] Furthermore, porosity Si 12 is removed alternatively. The fluoric acid which is the etching reagent of usual Si, or the selection etching reagent of Porosity Si, To fluoric acid, or alcohol and mixed liquor of hydrogen peroxide solution which added either at least, Or at least one kind of the mixed liquor of alcohol and hydrogen peroxide solution which added either at least is used for buffered fluoric acid or buffered fluoric acid. Non-electrolyzed wet chemical etching of the porosity Si 12 is carried out, and on insulating substrate 15 +14, the thin-film-ized single crystal Si layer 13 is made to remain, and it forms. As the detailed explanation was carried out [above-mentioned], it is possible for the etching reagent of usual Si to also etch Porosity Si alternatively with the huge surface area of Porosity Si.
[0053] Or porosity Si 12 is removed by selection polish by using the single crystal Si layer 13 as a polish stopper.
[0054] The semi-conductor substrate obtained by this invention is shown in drawing 1 (e). The semi-conductor substrate which lamination is carried out evenly [the single crystal Si layer 13] to homogeneity, and is formed throughout a wafer on insulating substrate 15 +14 at a large area and which was obtained in this way can be suitably used, even if it sees from the point of electronic device production by which insulating separation was carried out.
[0055] 1st Si single crystal substrate 11 removes the residual porosity Si, and when ruined so that surface surface smoothness is nonpermissible, after it performs surface flattening, it is again used for it as 1st Si single crystal substrate 11.
[0056] The approach of pressurizing from the both sides of the base stuck as an approach of separating two bases in a porosity Si layer in this invention, and crushing a porous layer, and each base are lengthened on both sides, and the approach of separating both, the method of inserting a fixture to a porous layer, the method of applying the force in the direction parallel to the front face of the stuck base, the method of adding supersonic vibration to a porous layer, etc. can be adopted.
[0057] In this invention, generally the porosity (porosity) of the porosity Si layer suitable for separation is 10 - 80% of range, and is 20 - 60% of range more preferably.
[0058] As shown in [example 2 of embodiment] drawing 2 (a), 1st Si single crystal substrate 21 is prepared first, the surface layer is carried out porosity-ized 22, and the nonvesicular single crystal Si layer 23 is formed on porosity Si 22 (drawing 2 (b)).
[0059] Next, as shown in drawing 2 (c), after sticking the light transmission nature support substrate 24 and the single crystal Si layer 23 which are represented by a quartz and glass at a room temperature through an insulating layer 25, it sticks with anode plate junction, pressurization, heat treatments, or such combination. This combines firmly the light transmission nature support substrate 24 and the single crystal layer 23 through an insulating layer 25. Or it forms an insulating layer 25 at least in one side on a single crystal Si layer and the light transmission nature support substrate 24, it is stuck by the three-sheet pile on both sides of insulating sheet metal.
[0060] Next, a substrate is divided in the porosity Si layer 23 (drawing 2 (d)). A light transmission nature support substrate side serves as structure like the 25/light transmission nature support substrate 24

of 23/insulating layers of porosity Si22/single crystal Si layers.
[0061] Furthermore, porosity Si 22 is removed alternatively. The fluoric acid which is the etching reagent of usual Si, or the selection etching reagent of Porosity Si, To fluoric acid, or alcohol and mixed liquor of hydrogen peroxide solution which added either at least, Or at least one kind of the mixed liquor of alcohol and hydrogen peroxide solution which added either at least is used for buffered fluoric acid or buffered fluoric acid. Non-electrolyzed wet chemical etching of the porosity Si 22 is carried out, and on light transmission nature insulation substrate 25 +24, the thin-film-ized single crystal Si layer 23 is made to remain, and it forms. As the detailed explanation was carried out [above-mentioned], it is possible for the etching reagent of usual Si to also etch Porosity Si alternatively with the huge surface area of Porosity Si.
[0062] Or porosity Si 22 is removed by sorting polish by using the single crystal Si layer 23 as a polish stopper.
[0063] The semi-conductor substrate obtained by this invention is shown in drawing 2 (e). On light transmission nature insulation base 25 +24, evenly, lamination of the single crystal Si layer 23 is carried out to homogeneity, and it is formed throughout a wafer at a large area. In this way, the obtained semi-conductor substrate can be suitably used, even if it sees from the point of electronic device production by which insulating separation was carried out.
[0064] There may not be the insulating mediation layer 25.
[0065] 1st Si single crystal substrate 21 removes the residual porosity Si, and when ruined so that surface surface smoothness is nonpermissible, after it performs surface flattening, it can be again used for it as 1st Si single crystal substrate 21.
[0066] As shown in [example 3 of embodiment] drawing 3 (a), 1st Si single crystal substrate 31 is prepared first, the surface layer is carried out porosity-ized 32, and the nonvesicular single crystal compound semiconductor layer 33 is formed on porosity Si 32 (drawing 3 (b)).
[0067] Next, as shown in drawing 3 (c), after sticking another Si support substrate 34 and single crystal compound semiconductor layer 33 at a room temperature through an insulating layer 35, it sticks with anode plate junction, pressurization, heat treatments, or such combination. This combines firmly Si support substrate 34 and the single crystal layer 33 through an insulating layer 35. Three insulating layers 35 are stuck in piles on both sides of insulating sheet metal, or it forms at least in one side on a single crystal compound semiconductor layer and Si support substrate 34.
[0068] Next, a substrate is divided in the porosity Si layer 32 (drawing 3 (d)). Si support substrate side serves as structure like the 35/Si support substrate 34 of 33/insulating layers of porosity Si32/single crystal compound semiconductor layers.
[0069] Furthermore, porosity Si 32 is removed alternatively. Chemical etching of the porosity Si 32 is carried out using an etching reagent with the early etch rate of Si to a compound semiconductor, and on insulating substrate 35 +34, the thin-film-ized single crystal compound semiconductor layer 33 is made to remain, and it forms.
[0070] Or porosity Si 32 is removed by selection polish by using the single crystal compound semiconductor layer 33 as a polish stopper.
[0071] The semi-conductor substrate obtained by this invention is shown in drawing 3 (e). On insulating substrate 35 +34, evenly, lamination of the single crystal compound semiconductor layer 33 is carried out to homogeneity, and it is formed throughout a wafer at a large area. In this way, the obtained semi-conductor substrate can be suitably used, even if it sees as a compound semiconductor substrate from the point of electronic device production by which insulating separation was carried out further.
[0072] When using as a compound semiconductor substrate, there may not be an insulating layer 35.
[0073] 1st Si single crystal substrate 31 removes the residual porosity Si, and when ruined so that surface surface smoothness is nonpermissible, after it performs surface flattening, it can be again used for it as 1st Si single crystal substrate 31.
[0074] As shown in [example 4 of embodiment] drawing 4 (a), 1st Si single crystal substrate 41 is prepared first, the surface layer is carried out porosity-ized 42, and the nonvesicular single crystal compound semiconductor layer 43 is formed on porosity Si 42 (drawing 4 (b)).

[0075] Next, as shown in drawing 4 (c), after sticking the light transmission nature support substrate 44 and the single crystal compound semiconductor layer 43 which are represented by a quartz and glass at a room temperature through an insulating layer 45, it sticks with anode plate junction, pressurization, heat treatments, or such combination. This combines firmly the light transmission nature support substrate 44 and the single crystal layer 43 through an insulating layer 45. Or it forms an insulating layer 45 at least in one side on a single crystal compound semiconductor layer and the light transmission nature support substrate 44, it is stuck by the three-sheet pile on both sides of insulating sheet metal.
[0076] Next, a substrate is divided in the porosity Si layer 43 (drawing 4 (d)). A light transmission nature support substrate side serves as structure like the 45/light transmission nature support substrate 44 of 43/insulating layers of porosity Si42/single crystal compound semiconductor layers.
[0077] Furthermore, porosity Si 42 is removed alternatively. Chemical etching of the porosity Si 42 is carried out using an etching reagent with the quick etch rate of Si to a compound semiconductor, and on insulating substrate 45 +44, the thin-film-ized single crystal compound semiconductor layer 43 is made to remain, and it forms.
[0078] Or porosity Si 42 is removed by selection polish by using the single crystal compound semiconductor layer 43 as a polish stopper.
[0079] The semi-conductor substrate obtained by this invention is shown in drawing 4 (e). On light transmission nature insulation substrate 45 +44, evenly, lamination of the single crystal compound semiconductor layer 43 is carried out to homogeneity, and it is formed throughout a wafer at a large area. In this way, the obtained semi-conductor substrate can be suitably used, even if it sees from the point of electronic device production by which insulating separation was carried out.
[0080] There may not be the insulating mediation layer 45.
[0081] 1st Si single crystal substrate 41 removes the residual porosity Si, and when ruined so that surface surface smoothness is nonpermissible, after it performs surface flattening, it can be again used for it as 1st Si single crystal substrate 41.
[0082] it is shown in [example 5 of embodiment] drawing 5 (a) -- as -- first -- 1st Si single crystal substrate 51 -- preparing -- the surface layer of the both sides -- the porosity-izing 52 -- 53 are taken and the nonvesicular single crystal half conductor layers 54 and 55 are formed on the double-sided porosity Si 52 and 53 (drawing 5 (b)).
[0083] Next, as shown in drawing 5 (c), after sticking two support substrates 56 and 57 and the single crystal half conductor layers 54 and 55 at a room temperature through insulating layers 58 and 59, respectively, it sticks with anode plate junction, pressurization, heat treatments, or such combination. This combines firmly the support substrates 56 and 57 and the single crystal layers 54 and 55 through insulating layers 58 and 59. Or it forms insulating layers 58 and 59 at least in one side on the support substrate 56 and 67 on the single crystal half conductor layer 54 and 55, they are stuck by the five-sheet pile on both sides of insulating sheet metal.
[0084] Next, a substrate is trichotomized in both the porosity Si layers 52 and 53 (drawing 5 (d)). Two support substrates serve as structure like porosity Si / single crystal half conductor layer / insulating layer / support substrate (52/54/58/56, and 53/55/59/57).
[0085] Furthermore, both the porosity 52 and Si 53 is removed alternatively. Chemical etching of the porosity 52 and Si 53 is carried out alternatively, and on the support substrates 58/56, and 59/57, the thin-film-ized single crystal half conductor layers 54 and 55 are made to remain, and it forms.
[0086] Or porosity 52 and Si 53 is removed by selection and polish by using the single crystal half conductor layers 54 and 55 as a polish stopper.
[0087] The semi-conductor substrate obtained by this invention is shown in drawing 5 (e). On a support substrate, evenly, lamination of the single crystal compound semiconductor layer is carried out to homogeneity, and it is formed throughout a wafer at two-body coincidence at a large area. In this way, the obtained semi-conductor substrate can be suitably used, even if it sees from the point of electronic device production by which insulating separation was carried out.
[0088] There may not be the insulating mediation layers 58 and 59.
[0089] The support substrates 56 and 57 may not be the same.

[0090] 1st Si single crystal substrate 51 removes the residual porosity Si, and when ruined so that surface surface smoothness is nonpermissible, after it performs surface flattening, it can be again used for it as 1st Si single crystal 51.
[0091]
[Example]
(Example 1) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 6 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm into HF solution.
[0092] The anodization conditions were as follows.
[0093] Current density: 5 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:1:1 hour: -- 12 (minute)
Thickness of Porosity Si: 10 (micrometer)
Porosity:15(%)
This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- CVD (ChemicalVapor Deposition) -- 1 micrometer grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0094] source gas: -- SiH2 Cl2 / H2 quantity-of-gas-flow: -- 0.5/180 l/min gas pressure: -- 80Torr temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.
[0095] This SiO2 500nm SiO2 prepared apart from the layer front face Superposition and after making it contact, heat treatment of 900 degrees C - 2 hours was carried out for the front face of Si substrate in which the layer was formed, and lamination was performed.
[0096] When sufficient hauling force for homogeneity was perpendicularly applied to the field of the stuck wafer, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it. Adhesives were used, the plate was specifically pasted up on both sides of the stuck wafer, and after arranging this plate on the fixture made to move in the direction which pulls apart this plate of each other, it was pulled apart in two.
[0097] Then, selective etching was carried out, agitating a porosity Si layer 49% with the mixed liquor (1:5) of fluoric acid and 30% hydrogen peroxide solution. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal Si was removed completely.
[0098] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, the selection ratio with the etch rate of a porous layer amounts to the fifth power or more of 10, and the amount of etching in a nonvesicular layer (about dozens of A) is thickness reduction which can be disregarded practically.
[0099] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.
[0100] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0101] In this way, the SOI substrate which has a quality semi-conductor layer was obtained. Furthermore, after the same etching removed the porous layer which remains in Si substrate of another side separated bordering on the porosity Si layer, polishing of the front face was carried out. In this way, the SOI substrate plurality which has a quality semi-conductor layer was obtained by repeating an above-mentioned process using obtained Si substrate.
[0102] (Example 2) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 4 inch of the P type with the thickness of 525 micrometers of specific resistance 0.01 ohm-cm into HF solution.
[0103] The anodization conditions were as follows.
[0104] Current density: 7 (mA-cm -2)

anodization solution: -- HF:H2 O:C2 H5 OH=1:1:1 hour: -- 12 (minute)
Thickness of Porosity Si: 10 (micrometer)
Porosity:15(%)
This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 2 hours. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- MBE (Molecular Beam Epitaxy) -- 0.5 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0105] temperature: -- 700-degree-C pressure: -- 1x10-9Torr growth rate: -- 0.1 nm/sec temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.
[0106] This SiO2 Superposition and after making it contact, heat treatment of 400 degrees C - 2 hours was carried out for the layer front face and the front face of the fused-quartz substrate prepared independently, and lamination was performed.
[0107] When sufficient pressure for homogeneity was perpendicularly applied to the field of the stuck wafer, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it. Adhesives were used, the plate was specifically pasted up on both sides of the stuck wafer, and after arranging this plate on the fixture which stated this plate in the example 1, Si layer was destroyed by applying a pressure to this plate.
[0108] Then, selective etching is carried out, agitating a porosity Si layer with the mixed liquor (1:5) of buffered fluoric acid and 30% hydrogen peroxide solution. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal Si was removed completely.
[0109] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, the selection ratio with the etch rate of a porous layer amounts to the fifth power or more of 10, and the amount of etching in a nonvesicular layer (about dozens of A) is thickness reduction which can be disregarded practically.
[0110] That is, the single crystal Si layer which had the thickness of 0.5 micrometers on the fused-quartz substrate has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.
[0111] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0112] The SOI substrate plurality which has a quality semi-conductor layer by repeating an above-mentioned process like an example 1 was obtained.
[0113] (Example 3) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 6 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.
[0114] The anodization conditions were as follows.
[0115] Current density: 7 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:1:1 hour: -- 12 (minute)
Thickness of Porosity Si: 10 (micrometer)
Porosity:15(%)
This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- MOCVD (MetalOrganic Chemical Vapor Deposition) -- 1 micrometer grew the single crystal GaAs epitaxially by law. The growth conditions are as follows.
[0116] source gas: -- TMG/AsH3 / H2 gas-pressure: -- 80Torr temperature: -- superposition and after making it contact, heat treatment of 900 degrees C - 1 hour was carried out for 700-degree-C this GaAs layer front face and the front face of 2nd Si substrate prepared independently, and lamination was performed. Both substrates were firmly stuck by this heat treatment.
[0117] When the pressure was applied to the stuck wafer like the example 2, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it.

[0118] Then, after removing the oxide film of a wall for a porosity Si layer by fluoric acid, Porosity Si was etched by 110 degrees C (ratio of 17ml : 3g : 8ml) of ethylenediamine + pyrocatechol + water. The single crystal GaAs remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal GaAs was removed completely.
[0119] The etch rate to this etching reagent of a single crystal GaAs is very low, and is thickness reduction which can be disregarded practically.
[0120] That is, the single crystal GaAs layer which had the thickness of 1 micrometer on Si substrate has been formed. It was changeless in a single crystal GaAs layer in any way also by the selective etching of Porosity Si.
[0121] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into a GaAs layer, but it was checked that good crystallinity is maintained.
[0122] Like the example 2, the above-mentioned process was repeated and two or more semi-conductor substrates which allotted the quality GaAs layer were obtained.
[0123] By using Si substrate with an oxide film as a support substrate, GaAs on an insulator layer was producible similarly.
[0124] (Example 4) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 5 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.
[0125] The anodization conditions were as follows.
[0126] Current density: 10 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:1:1 hour: -- 24 (minute)
Thickness of Porosity Si: 20 (micrometer)
Porosity:17(%)
This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 2 hours. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- MBE (Molecular Beam Epitaxy) -- 0.5 micrometers grew the single crystal AlGaAs epitaxially by law.
[0127] Superposition and after making it contact, heat treatment of 500 degrees C - 2 hours was carried out for this AlGaAs layer front face and the front face of the low-melting-glass substrate prepared independently, and lamination was performed. Both substrates were firmly stuck by this heat treatment.
[0128] When the pressure was applied like the stuck wafer example 2, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it.
[0129] Then, Porosity Si was etched with the fluoric acid solution. The single crystal AlGaAs remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal AlGaAs was removed completely.
[0130] The etch rate to this etching reagent of a single crystal AlGaAs is very low, and is thickness reduction which can be disregarded practically.
[0131] That is, the single crystal AlGaAs layer which had the thickness of 0.5 micrometers on the glass substrate has been formed. It was changeless in a single crystal AlGaAs layer in any way also by the selective etching of Porosity Si.
[0132] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into an AlGaAs layer, but it was checked that good crystallinity is maintained. Two or more substrates which have a quality semi-conductor layer by repeating an above-mentioned process like an example 2 were obtained.
[0133] (Example 5) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 6 inch of double-sided polish of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type to both sides into HF solution.
[0134] The anodization conditions were as follows.
[0135] Current density: 5 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:1:1 hour: -- 12x2 (minute)

Thickness of Porosity Si: Each 10 (micrometer)
Porosity:15(%)
This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. the porosity Si top formed in both sides -- CVD (Chemical Vapor Deposition) -- 1 micrometer grew the single crystal Si epitaxially by law, respectively. The growth conditions are as follows.
[0136] source gas: -- SiH2 Cl2 / H2 quantity-of-gas-flow: -- 0.5/180 l/min gas pressure: -- 80Torr temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.
[0137] This SiO2 500nm SiO2 prepared apart from the layer front face Superposition and after making it contact, heat treatment of 600 degrees C - 2 hours was carried out for the front face of two Si substrates in which the layer was formed, respectively, and lamination was performed.
[0138] When perpendicularly sufficient hauling force was applied to the field of the wafer stuck using the technique of an example 1, the porosity Si layer destroyed two-layer, the wafer was trichotomized and Porosity Si expressed it.
[0139] Then, selective etching is carried out, agitating a porosity Si layer 49% with the mixed liquor (1:5) of fluoric acid and 30% hydrogen peroxide solution. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal Si was removed completely.
[0140] the etch rate to this etching reagent of a nonvesicular Si single crystal -- very -- low -- the selection ratio with the etch rate of a porous layer -- the fifth power or more of 10 -- reaching -- a ratio -- the amount of etching in a porous layer (about dozens of A) is thickness reduction which can be disregarded practically.
[0141] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has formed in two-sheet coincidence. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.
[0142] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained. The above-mentioned process as well as an example 1 was repeated, and the substrate plurality which has a quality semi-conductor layer was obtained.
[0143] (Example 6) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 5 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.
[0144] The anodization conditions were as follows.
[0145] Current density: 7 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:1:1 hour: -- 4 (minute)
Thickness of Porosity Si: 3 (micrometer)
Porosity:15(%)
Furthermore, current density: 30 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:3:2 hour: -- 3 (minute)
Thickness of Porosity Si: 10 (micrometer)
Porosity:45(%)
This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. 0.3 micrometers grew the single crystal Si epitaxially with the CVD method on Porosity Si. The growth conditions are as follows.
[0146] source gas: -- SiH4 carrier gas: -- H2 temperature: -- 850-degree-C pressure: -- 1x10-2Torr growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation further 3.3 nm/sec.
[0147] This SiO2 500nm SiO2 prepared apart from the layer front face Superposition and after making it contact, heat treatment of 700 degrees C - 2 hours was carried out for the front face of Si substrate in

which the layer was formed, and lamination was performed.
[0148] The porosity Si layer broke in the place which applied perpendicularly sufficient hauling force to the field of the stuck wafer using the technique of an example 1, the wafer was halved and Porosity Si expressed it.
[0149] Then, selective etching of the porosity Si layer is carried out with the etching reagent of HF/HNO3 / CH3 COOH system. Porosity Si was etched and was removed completely.
[0150] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, and the amount of etching in a nonvesicular layer is thickness reduction which can be disregarded practically.
[0151] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.
[0152] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained. The above-mentioned process as well as an example 1 was repeated, and the substrate plurality which has a quality semi-conductor layer was obtained.
[0153] (Example 7) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 6 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.
[0154] The anodization conditions were as follows.
[0155] Current density: 5 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:1:1 hour: -- 12 (minute)
Thickness of Porosity Si: 10 (micrometer)
Porosity:15(%)
This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- CVD (ChemicalVapor Deposition) -- 1 micrometer grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0156] source gas: -- SiH2 Cl2 / H2 quantity-of-gas-flow: -- 0.5/180 l/min gas pressure: -- 80Torr temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.
[0157] This SiO2 500nm SiO2 prepared apart from the layer front face Superposition and after making it contact, heat treatment of 900 degrees C - 2 hours was carried out for the front face of Si substrate in which the layer was formed, and lamination was performed.
[0158] When perpendicularly sufficient hauling force was applied to the field of the stuck wafer using the technique of an example 1, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it.
[0159] Then, selection polish of the porosity Si layer was carried out, having used the single crystal Si as the stopper. Porosity Si selection polish was carried out and it was removed completely.
[0160] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.
[0161] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained. The above-mentioned process as well as an example 1 was repeated, and the substrate plurality which has a quality semi-conductor layer was obtained.
[0162] (Example 8) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 6 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.
[0163] The anodization conditions were as follows.
[0164] Current density: 5 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:1:1 hour: -- 12 (minute)

Thickness of Porosity Si: 10 (micrometer)
Porosity:15(%)
This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- CVD (ChemicalVapor Deposition) -- 1 micrometer grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0165] source gas: -- SiH2 Cl2 / H2 quantity-of-gas-flow: -- 0.5/180 l/min gas pressure: -- 80Torr temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.
[0166] This SiO2 500nm SiO2 prepared apart from the layer front face Superposition and after making it contact, heat treatment of 900 degrees C - 2 hours was carried out for the front face of Si substrate in which the layer was formed, and lamination was performed. Subsequently, when the stuck substrate was put in into the layer which arranged the ultrasonic vibrator and ultrasonic energy was impressed, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it.
[0167] Then, selective etching is carried out, agitating a porosity Si layer 49% with the mixed liquor (1:5) of fluoric acid and 30% hydrogen peroxide solution. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal Si was removed completely.
[0168] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, the selection ratio with the etch rate of a porous layer amounts to the fifth power or more of 10, and the amount of etching in a nonvesicular layer (about dozens of A) is thickness reduction which can be disregarded practically.
[0169] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.
[0170] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0171] 1st Si single crystal substrate removed the residual porosity Si, and used it as 1st Si single crystal substrate again.
[0172] (Example 9) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 4 inch of the P type with the thickness of 525 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.
[0173] The anodization conditions were as follows.
[0174] Current density: 7 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:1:1 hour: -- 12 (minute)
Thickness of Porosity Si: 10 (micrometer)
Porosity:15(%)
This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 2 hours. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- MBE (Molecular Beam Epitaxy) -- 0.5 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0175] temperature: -- 700-degree-C pressure: -- 1x10-9Torr growth rate: -- 0.1 nm/sec temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.
[0176] This SiO2 Superposition and after making it contact, heat treatment of 400 degrees C - 2 hours was carried out for the layer front face and the front face of the fused-quartz substrate prepared independently, and lamination was performed.
[0177] The wafer end face was made to express a porous layer, when Porosity Si was etched to some extent and the sharp plate was inserted there like the cutting edge of a razor, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it.
[0178] Then, selective etching is carried out, agitating a porosity Si layer with the mixed liquor (1:5) of

buffered fluoric acid and 30% hydrogen peroxide solution. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal Si was removed completely.
[0179] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, the selection ratio with the etch rate of a porous layer amounts to the fifth power or more of 10, and the amount of etching in a nonvesicular layer (about dozens of A) is thickness reduction which can be disregarded practically.
[0180] That is, the single crystal Si layer which had the thickness of 0.5 micrometers on the fused-quartz substrate has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.
[0181] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0182] The same result was obtained even if it did not form an oxide film in the epitaxial Si layer front face.
[0183] 1st Si single crystal substrate removed the residual porosity Si, and after performing surface polish and making it the shape of a mirror plane, it used it as 1st Si single crystal substrate again.
[0184] (Example 10) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 6 inch of double-sided polish of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type to both sides into HF solution.
[0185] The anodization conditions were as follows.
[0186] Current density: 5 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:1:1 hour: -- 12x2 (minute)
Thickness of Porosity Si: Each 10 (micrometer)
Porosity:15(%)
This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. the porosity Si top formed in both sides -- CVD (Chemical Vapor Deposition) -- 1 micrometer grew the single crystal Si epitaxially by law. The growth conditions are as follows.
[0187] source gas: -- SiH2 Cl2 / H2 quantity-of-gas-flow: -- 0.5/180 l/min gas pressure: -- 80Torr temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.
[0188] This SiO2 500nm SiO2 prepared apart from the layer front face Superposition and after making it contact, heat treatment of 600 degrees C - 2 hours was carried out for the front face of two Si substrates in which the layer was formed, respectively, and lamination was performed.
[0189] After making the wafer end face express a porous layer and infiltrating liquids, such as water, into a porous layer Si, when the whole lamination wafer was heated or cooled, the porosity Si layer broke by expansion of a liquid etc., the wafer was halved and Porosity Si expressed it.
[0190] Then, selective etching is carried out, agitating a porosity Si layer 49% with the mixed liquor (1:5) of fluoric acid and 30% hydrogen peroxide solution. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal Si was removed completely.
[0191] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, the selection ratio with the etch rate of a porous layer amounts to the fifth power or more of 10, and the amount of etching in a nonvesicular layer (about dozens of A) is thickness reduction which can be disregarded practically.
[0192] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has formed in two-sheet coincidence. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.
[0193] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0194] The same result was obtained even if it did not form an oxide film in the epitaxial Si layer front

face.
[0195] 1st Si single crystal substrate removed the residual porosity Si, and after it carried out hydrogen processing and carried out flattening of the front face, it used it as 1st Si single crystal substrate again.
[0196] (Example 11) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 5 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.
[0197] The anodization conditions were as follows.
[0198] Current density: 7 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:1:1 hour: -- 4 (minute)
Thickness of Porosity Si: 3 (micrometer)
Porosity:15(%)
Furthermore, current density: 30 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:3:2 hour: -- 3 (minute)
Thickness of Porosity Si: 10 (micrometer)
Porosity:45(%)
This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. 0.3 micrometers grew the single crystal Si epitaxially with the CVD method on Porosity Si. The growth conditions are as follows.
[0199] source gas: -- SiH4 carrier gas: -- H2 temperature: -- 850-degree-C pressure: -- 1x10-2Torr growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation further 3.3 nm/sec.
[0200] This SiO2 500nm SiO2 prepared apart from the layer front face Superposition and after making it contact, heat treatment of 700 degrees C - 2 hours was carried out for the front face of Si substrate in which the layer was formed, and lamination was performed.
[0201] When the force was horizontally applied to the 2nd (or the 1st) substrate to the 1st (or the 2nd) substrate, a porosity Si layer could not finish bearing shearing stress, and it destroyed, and the wafer was halved and Porosity Si expressed it.
[0202] Then, selective etching of the porosity Si layer is carried out with the etching reagent of HF/HNO3 / CH3 COOH system. Selective etching of the porosity Si was carried out, and it was removed completely.
[0203] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, and the amount of etching in a nonvesicular layer is thickness reduction which can be disregarded practically.
[0204] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.
[0205] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0206] The same result was obtained even if it did not form an oxide film in the epitaxial Si layer front face.
[0207] 1st Si single crystal substrate removed the residual porosity Si, and used it as 1st Si single crystal substrate again.
[0208] (Example 12) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 5 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.
[0209] The anodization conditions were as follows.
[0210] Current density: 7 (mA-cm -2)
anodization solution: -- HF:H2 O:C2 H5 OH=1:1:1 hour: -- 4 (minute)
Thickness of Porosity Si: 3 (micrometer)
Porosity:15(%)
Furthermore, current density: 30 (mA-cm -2)

anodization solution: -- HF:H2 O:C2 H5 OH=1:3:2 hour: -- 3 (minute)
Thickness of Porosity Si: 10 (micrometer)
Porosity:45(%)
This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. 0.3 micrometers grew the single crystal Si epitaxially with the CVD method on Porosity Si. The growth conditions are as follows.
[0211] source gas: -- SiH4 carrier gas: -- H2 temperature: -- 850-degree-C pressure: -- 1x10-2Torr growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation further 3.3 nm/sec.
[0212] This SiO2 500nm SiO2 prepared apart from the layer front face Superposition and after making it contact, heat treatment of 700 degrees C - 2 hours was carried out for the front face of Si substrate in which the layer was formed, and lamination was performed.
[0213] The wafer end face was made to express a porous layer, and the wafer was halved when the porosity Si layer was etched from the end face with the selection etching reagent of Porosity Si.
[0214] Then, selective etching of the porosity Si layer is carried out with the etching reagent of HF/HNO3 / CH3 COOH system. Selective etching of the porosity Si was carried out, and it was removed completely.
[0215] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, and the amount of etching in a nonvesicular layer is thickness reduction which can be disregarded practically.
[0216] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.
[0217] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.
[0218] The same result was obtained even if it did not form an oxide film in the epitaxial Si layer front face.
[0219] 1st Si single crystal substrate removed the residual porosity Si, and used it as 1st Si single crystal substrate again.
[0220]
[Effect of the Invention] As explained above, according to this invention, it sticks, the constituted base is separated by the porous layer, and the semi-conductor base with which the quality nonvesicular single crystal half conductor layer was allotted can be formed by removing the porous layer on the 2nd base to which the nonvesicular single crystal half conductor layer was allotted.
[0221] In addition, it sticks and the constituted base is separated by the porous layer, and since the 1st base from which the porous layer was removed by removing the porous layer which constitutes the 1st base is reusable to semi-conductor base production, improvement in the productivity of a semi-conductor base and low cost-ization can be attained further.
[0222] Moreover, according to this invention, the production approach of the semi-conductor substrate which stood high in the field of productivity, homogeneity, a controllability, and cost on substrates including a transparence substrate (light transmission nature substrate) when crystallinity obtained a single crystal layer or compound semiconductor single crystal layers, such as Si which was excellent just like the single crystal wafer, can be proposed.
[0223] Moreover, according to this invention, also in case the large-scale integrated circuit of SOI structure is produced, the production approach of expensive SOS and the alternative ********** substrate of SIMOX can be proposed.
[0224] Moreover, a base is separable into two or more through a porous layer, and after one base after separation removes residual porosity, it is usable as a semi-conductor substrate, and after removing residual porosity, it is applicable [the base of another side] to production of a semi-conductor substrate according to this invention, again.
[0225] Moreover, a porous layer and a nonvesicular single crystal layer are formed in both sides of a

base, and after sticking another base of two sheets so that this single crystal layer may be pinched, two semi-conductor substrates are producible to coincidence according to this invention, by separating a base by said porous layer.

[0226] namely, -- according to this invention -- economical efficiency -- excelling -- a large area -- crossing -- homogeneity -- it can leave the semi-conductor layer or compound semiconductor barrier layer formed in the front face using the flat single crystal substrate which has the extremely excellent crystallinity, this from the one side to barrier layer can be removed, and the production approach of a semi-conductor substrate of obtaining few remarkable single crystal layers or compound semiconductor crystal layer of a defect to an insulating lifter can be offered.

[0227] Moreover, the production approach of the semi-conductor substrate which stood high in the field of productivity, homogeneity, a controllability, and cost on the transparence substrate (light transmission nature substrate) when crystallinity obtained Si which was excellent just like the single crystal wafer, or a compound semiconductor single crystal layer can be acquired.

[0228] Moreover, also in case the large-scale integrated circuit of SOI structure is produced, the production approach of expensive SOS and the alternative ********** substrate of SIMOX can be acquired.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is a typical sectional view for explaining one example of the approach of this invention.
[Drawing 2] It is a typical sectional view for explaining one example of the approach of this invention.
[Drawing 3] It is a typical sectional view for explaining one example of the approach of this invention.
[Drawing 4] It is a typical sectional view for explaining one example of the approach of this invention.
[Drawing 5] It is a typical sectional view for explaining one example of the approach of this invention.
[Description of Notations]
11 Si Single Crystal Substrate
12 Porosity Si Layer
13 Nonvesicular Single Crystal Si Layer
14 Si Support Substrate
15 Insulating Layer

[Translation done.]

* NOTICES *

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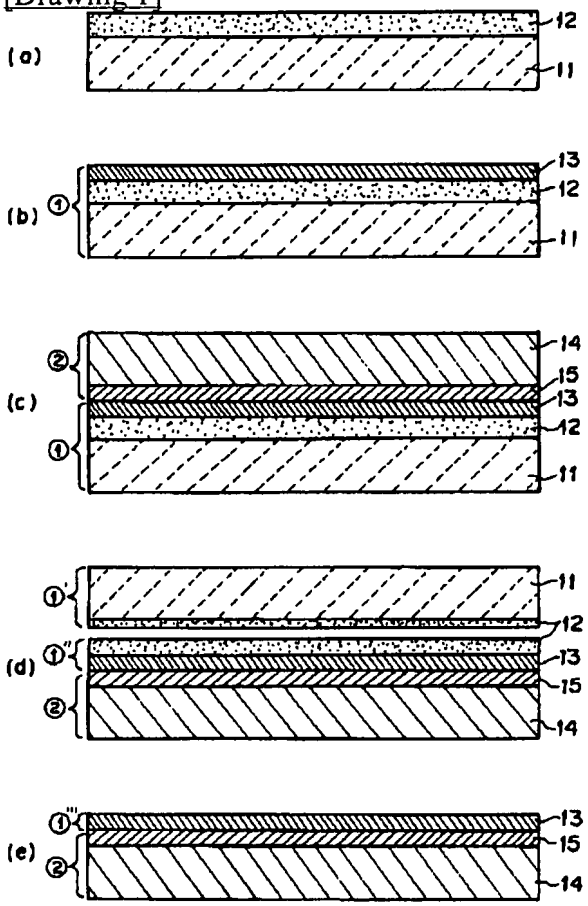
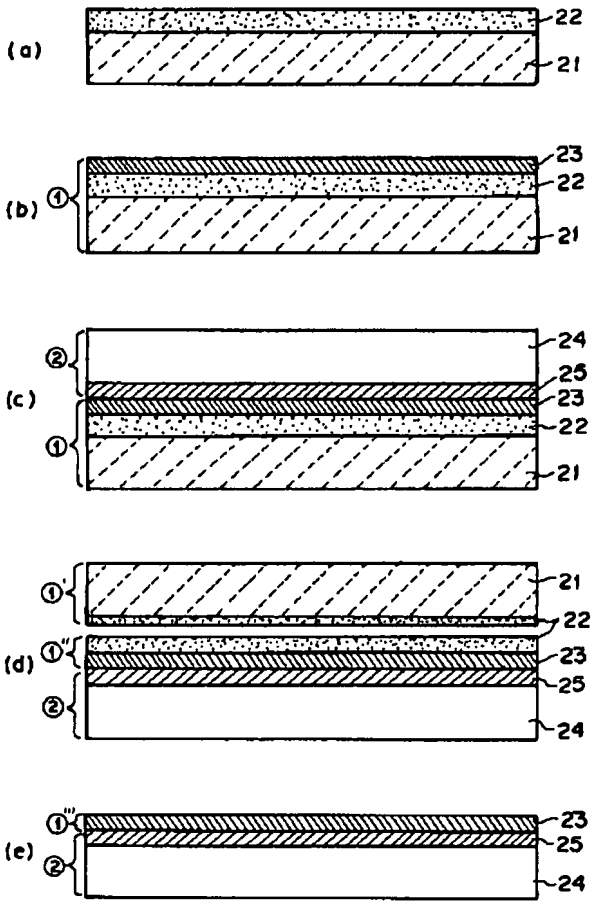
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

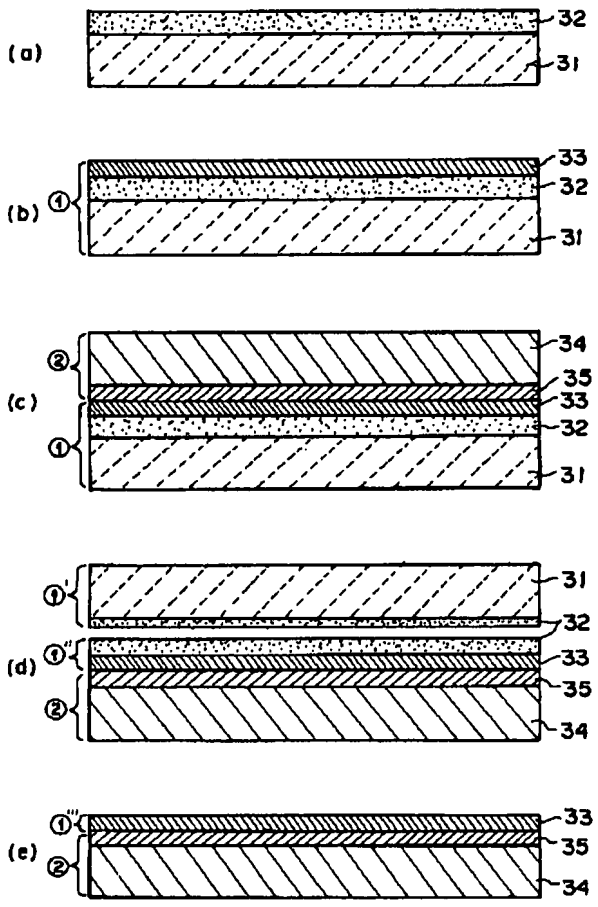
[Drawing 1]



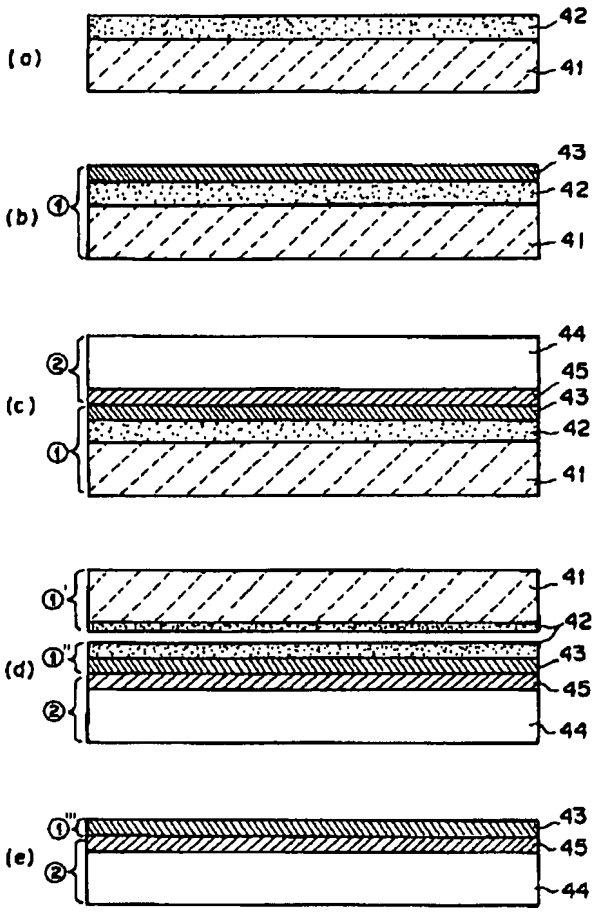
[Drawing 2]



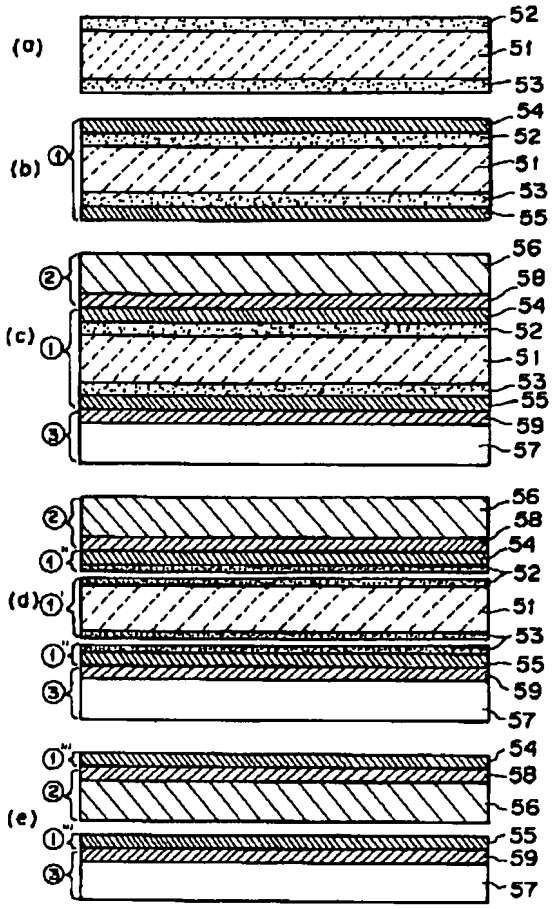
[Drawing 3]



[Drawing 4]



[Drawing 5]



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* NOTICES *

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23/12 D
23/14 C

[Procedure revision]
[Filing Date] August 17, Heisei 10
[Procedure amendment 1]
[Document to be Amended] Specification
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[Proposed Amendment]
[Claim(s)]
[Claim 1] The process which forms the 1st base which has a nonvesicular single crystal half conductor layer on the porosity semi-conductor layer on a nonvesicular substrate,
The lamination process which sticks said nonvesicular single crystal half conductor layer with the 2nd base,
The separation process which separates said 1st and 2nd stuck bases in said porosity semi-conductor layer,

The production approach of the semi-conductor substrate characterized by having the process which removes the porosity semi-conductor layer allotted on the 2nd [said] base obtained according to said separation process, and the process which removes the porosity semi-conductor layer which constitutes said 1st base obtained according to said separation process.
[Claim 2] The process which forms the 1st base which has a nonvesicular single crystal half conductor layer on the porosity semi-conductor layer on a nonvesicular substrate,
The lamination process which sticks said nonvesicular single crystal half conductor layer through the 2nd base and insulating layer,
The separation process which separates said 1st and 2nd stuck bases in said porosity semi-conductor layer,
The production approach of the semi-conductor substrate characterized by having the process which removes the porosity semi-conductor layer allotted on the 2nd [said] base obtained according to said separation process, and the process which removes the porosity semi-conductor layer which constitutes said 1st base obtained according to said separation process.
[Claim 3] Said porosity semi-conductor layer is the production approach of claim 1 constituted using silicon, or a semi-conductor substrate given in 2.
[Claim 4] The production approach of claim 1 by which the thermal oxidation film is formed in the wall of the hole of said porosity semi-conductor layer, or a semi-conductor substrate given in two.
[Claim 5] Said porosity semi-conductor layer is the production approach of claim 1 which is a layer with a mechanical strength weaker than said nonvesicular substrate, or a semi-conductor substrate given in two.
[Claim 6] The porosity of said porosity semi-conductor layer is the production approach of claim 1 in 10 - 80% of range, or a semi-conductor substrate given in 2.
[Claim 7] Said porosity semi-conductor layer is the production approach of claim 1 which has the two-layer field where porosity differs mutually, or a semi-conductor substrate given in two.
[Claim 8] The two-layer field where said porosity differs is the production approach of a semi-conductor substrate according to claim 7 with the porosity of the side near said nonvesicular substrate higher than the porosity of the side near said nonvesicular single crystal half conductor layer.
[Claim 9] The production approach of claim 1 which performs the process after said lamination process as the 1st base which newly forms a porosity semi-conductor layer in the base which removes the porosity semi-conductor layer which constitutes said 1st base after said separation process, and is obtained, and has said porosity semi-conductor layer for this in it, or a semi-conductor substrate given in 2.
[Claim 10] Said nonvesicular single crystal half conductor layer is the production approach of claim 1 which is Si layer, or a semi-conductor substrate given in 2.
[Claim 11] Said nonvesicular single crystal half conductor layer is the production approach of claim 1 which is a compound semiconductor layer, or a semi-conductor substrate given in 2.
[Claim 12] Said nonvesicular single crystal half conductor layer is the production approach of claim 1 formed of epitaxial growth, or a semi-conductor substrate given in two.
[Claim 13] Said nonvesicular single crystal half conductor layer is the production approach of claim 1 formed by the approach chosen from the molecular-beam epitaxial method, a plasma-CVD method, a reduced pressure CVD method, an optical CVD method, a bias sputtering technique, and a liquid phase grown method, or a semi-conductor substrate given in two.
[Claim 14] Said 1st base is the production approach of claim 1 constituted using Si, or a semi-conductor substrate given in 2.
[Claim 15] Said 2nd base is the production approach of claim 1 which is a light transmission nature base, or a semi-conductor substrate given in 2.
[Claim 16] Removal of said porosity semi-conductor layer is the production approach of claim 1 made using etching, or a semi-conductor substrate given in 2.
[Claim 17] Removal of said porosity semi-conductor layer is the production approach of claim 1 made by grinding alternatively said nonvesicular single crystal half conductor layer for said porosity semi-

conductor layer as a stopper, or a semi-conductor substrate given in 2.
[Claim 18] Removal of said porosity semi-conductor layer is the production approach of claim 1 removed by chemical etching at fluoric acid or fluoric acid by the mixed liquor of alcohol and hydrogen peroxide solution which added either at least, or a semi-conductor substrate given in two.
[Claim 19] Said porosity semi-conductor layer is the production approach of claim 1 removed by chemical etching at buffered fluoric acid or buffered fluoric acid by the mixed liquor of alcohol and hydrogen peroxide solution which added either at least, or a semi-conductor substrate given in two.
[Claim 20] The separation in said porosity semi-conductor layer is the production approach of claim 1 performed by at least one or more approaches of pressurizing in the perpendicular direction to the lamination side of the stuck base, pulling in the direction perpendicular to said field, and applying-to this lamination side-shearing stress **, or a semi-conductor substrate given in 2.
[Claim 21] Said insulating layer is the production approach of the semi-conductor substrate according to claim 2 formed at least in one side on the front face of said 2nd base on said nonvesicular single crystal layer.
[Claim 22] Said insulating layer is the thermal oxidation film and deposition SiO2. The film and deposition Si3 N4 The production approach of the semi-conductor substrate according to claim 21 chosen from film.
[Claim 23] Said lamination process is the production approach of the semi-conductor substrate according to claim 1 or 2 performed by anode plate junction, pressurization, heat treatment, or the approach chosen from such combination.
[Claim 24] Said porosity semi-conductor layer is the production approach of the semi-conductor substrate according to claim 1 or 2 formed using anodization.
[Claim 25] Said anodization is the production approach of the semi-conductor substrate according to claim 24 performed in HF solution.
[Claim 26] Said anodization is the production approach of the semi-conductor substrate according to claim 24 performed according to the process which carries out anodization by the low current consistency, and the process which carries out anodization with high current density after that.
[Claim 27] The production approach of a semi-conductor substrate according to claim 26 with the concentration of HF in the process which carries out anodization by said low current consistency deeper than the concentration of HF in the process which carries out anodization with said high current density.
[Claim 28] The separation in said porosity semi-conductor layer is the production approach of claim 1 performed by impressing wave energy to this porosity semi-conductor layer, or a semi-conductor substrate given in 2.
[Claim 29] The separation in said porosity semi-conductor layer is the production approach of claim 1 performed by inserting the member for exfoliation from this porosity semi-conductor layer side face, or a semi-conductor substrate given in 2.
[Claim 30] The separation in said porosity semi-conductor layer is the production approach of claim 1 performed by the expansion energy of the matter into which this porosity semi-conductor layer was infiltrated, or a semi-conductor substrate given in 2.
[Claim 31] The separation in said porosity semi-conductor layer is the production approach of claim 1 performed by the selective etching to this porosity semi-conductor layer of a wafer side face, or a semi-conductor substrate given in 2.
[Claim 32] The semi-conductor substrate produced by the approach according to claim 1 to 31.
[Procedure amendment 2]
[Document to be Amended] Specification
[Item(s) to be Amended] 0032
[Method of Amendment] Modification
[Proposed Amendment]
[0032] Namely, the 1st mode of the production approach of the semi-conductor substrate of this invention The process which forms the 1st base which has a nonvesicular single crystal half conductor layer on the porosity semi-conductor layer on a nonvesicular substrate, The lamination process which

sticks said nonvesicular single crystal half conductor layer with the 2nd base, The separation process which separates said 1st and 2nd stuck bases in said porosity semi-conductor layer, It is characterized by having the process which removes the porosity semi-conductor layer allotted on the 2nd [said] base obtained according to said separation process, and the process which removes the porosity semi-conductor layer which constitutes said 1st base obtained according to said separation process.
[Procedure amendment 3]
[Document to be Amended] Specification
[Item(s) to be Amended] 0033
[Method of Amendment] Modification
[Proposed Amendment]
[0033] The process at which the 2nd mode of this invention forms the 1st base which has a nonvesicular single crystal half conductor layer on the porosity semi-conductor layer on a nonvesicular substrate, The lamination process which sticks said nonvesicular single crystal half conductor layer through the 2nd base and insulating layer, The separation process which separates said 1st and 2nd stuck bases in said porosity semi-conductor layer, It is characterized by having the process which removes the porosity semi-conductor layer allotted on the 2nd [said] base obtained according to said separation process, and the process which removes the porosity semi-conductor layer which constitutes said 1st base obtained according to said separation process.
[Procedure amendment 4]
[Document to be Amended] Specification
[Item(s) to be Amended] 0076
[Method of Amendment] Modification
[Proposed Amendment]
[0076] Next, a substrate is divided in the porosity Si layer 42 (drawing 4 (d)). A light transmission nature support substrate side serves as structure like the 45/light transmission nature support substrate 44 of 43/insulating layers of porosity Si42/single crystal compound semiconductor layers.
[Procedure amendment 5]
[Document to be Amended] Specification
[Item(s) to be Amended] 0166
[Method of Amendment] Modification
[Proposed Amendment]
[0166] This SiO2 500nm SiO2 prepared apart from the layer front face Superposition and after making it contact, heat treatment of 900 degrees C - 2 hours was carried out for the front face of Si substrate in which the layer was formed, and lamination was performed. Subsequently, when the stuck substrate was put in into the tub which arranged the ultrasonic vibrator and ultrasonic energy was impressed, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it.
[Procedure amendment 6]
[Document to be Amended] Specification
[Item(s) to be Amended] 0151
[Method of Amendment] Modification
[Proposed Amendment]
[0151] That is, the single crystal Si layer which had the thickness of 0.3 micrometers on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.
[Procedure amendment 7]
[Document to be Amended] Specification
[Item(s) to be Amended] 0204
[Method of Amendment] Modification
[Proposed Amendment]
[0204] That is, the single crystal Si layer which had the thickness of 0.3 micrometers on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of

Porosity Si.

[Translation done.]

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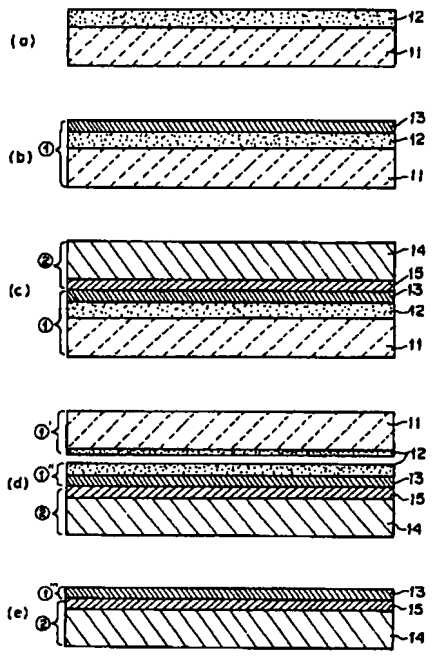
(54)【発明の名称】　半導体基板の作製方法

(57)【要約】

【目的】　光透過性基板等の絶縁性基板上に、結晶性が単結晶ウェハー並に優れたＳｉあるいは化合物半導体単結晶層を得るうえで、生産性、均一性、制御性、コストの面において卓越した半導体基板の作製方法を提案する。

【構成】　多孔質層１２を有する第１の基体１１の前記多孔質層１２上に非多孔質単結晶半導体層１３を形成する工程（ａ），（ｂ）、前記非多孔質単結晶半導体層１３を第２の基体（１４，１５）と貼り合わせる工程（ｃ）、前記貼り合わせて構成された基体を前記多孔質層１２において分離する工程（ｄ）、前記分離された第２の基体（１４，１５，１３）上に配された多孔質層１２を除去する工程（ｅ）、及び前記分離された第１の基体１１を構成する多孔質層１２を除去する工程を有することを特徴とする半導体基板の作製方法。



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【特許請求の範囲】

【請求項１】　多孔質層を有する第１の基体の前記多孔質層上に非多孔質単結晶半導体層を形成する工程、
前記非多孔質単結晶半導体層を第２の基体と貼り合わせる工程、
前記貼り合わせて構成された基体を前記多孔質層において分離する工程、
前記分離された第２の基体上に配された多孔質層を除去する工程、及び前記分離された第１の基体を構成する多孔質層を除去する工程を有することを特徴とする半導体基板の作製方法。

【請求項２】　多孔質層を有する第１の基体の前記多孔質層上に非多孔質単結晶半導体層を形成する工程、
前記非多孔質単結晶半導体層を第２の基体と絶縁層を介して貼り合わせる工程、
前記貼り合わせて構成された基体を前記多孔質層において分離する工程、
前記分離された第２の基体上に配された多孔質層を除去する工程、及び前記分離された第１の基体を構成する多孔質層を除去する工程を有することを特徴とする半導体基板の作製方法。

【請求項３】　前記多孔質層は、シリコンを用いて構成される請求項１あるいは請求項２に記載の半導体基板の作製方法。

【請求項４】　前記分離された第１の基体を構成する多孔質層を除去して得られる基体に、新たに多孔質層を形成し、これを前記多孔質層を有する第１の基体として前記貼り合わせ工程以降の工程を行なう請求項１あるいは請求項２に記載の半導体基板の作製方法。

【請求項５】　前記非多孔質単結晶半導体層は、Ｓｉ層である請求項１あるいは２に記載の半導体基板の作製方法。

【請求項６】　前記非多孔質単結晶半導体層は、化合物半導体層である請求項１あるいは２に記載の半導体基板の作製方法。

【請求項７】　前記第１の基体は、Ｓｉを用いて構成される請求項１あるいは２に記載の半導体基板の作製方法。

【請求項８】　前記第２の基体は、光透過性基体である請求項１あるいは２に記載の半導体基板の作製方法。

【請求項９】　前記多孔質層の除去はエッチングを用いてなされる請求項１あるいは２に記載の半導体基板の作製方法。

【請求項１０】　前記多孔質層の除去は、前記多孔質層を前記非多孔質単結晶半導体層をストッパーとして選択的に研磨することによりなされる請求項１あるいは２に記載の半導体基板の作製方法。

【請求項１１】　前記多孔質層における分離は、貼り合わせた基体の貼り合わせ面に対して垂直な方向に加圧すること、前記面に垂直な方向に引っ張ること、該貼合わ

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せ面に対して剪断応力をかけること、の少なくとも１つ以上の方法によって行われる請求項１あるいは２に記載の半導体基板の作製方法。

【請求項１２】　前記絶縁層は、前記非多孔質単結晶層上、前記第２の基体の表面上の少なくとも一方に形成する請求項２に記載の半導体基板の作製方法。

【請求項１３】　前記絶縁層は、熱酸化膜、堆積SiO_2膜、堆積Si_3N_4膜の中から選ばれる請求項１２に記載の半導体基板の作製方法。

【請求項１４】　前記貼り合わせ工程は、陽極接合、加圧、熱処理、あるいはこれらの組み合わせの中から選ばれた方法により行われる請求項１又は２に記載の半導体基板の作製方法。

【請求項１５】　前記多孔質層は、陽極化成を用いて形成される請求項１又は２記載の半導体基板の作製方法。

【請求項１６】　前記陽極化成は、ＨＦ溶液中で行われる請求項１５に記載の半導体基板の作製方法。

【請求項１７】　前記多孔質層における分離は、該多孔質層に波動エネルギーを印加することにより行われる請求項１あるいは２に記載の半導体基板の作製方法。

【請求項１８】　前記多孔質層における分離は、該多孔質層側面から剥離用部材を挿入することにより行われる請求項１あるいは２に記載の半導体基板の作製方法。

【請求項１９】　前記多孔質層における分離は、該多孔質層に染み込ませた物質の膨張エネルギーにより行われる請求項１あるいは２に記載の半導体基板の作製方法。

【請求項２０】　前記多孔質層における分離は、ウエハ側面の該多孔質層に対する選択エッチングにより行われる請求項１あるいは２に記載の半導体基板の作製方法。

【請求項２１】　前記多孔質層の多孔度は、１０～８０％の範囲にある請求項１あるいは２に記載の半導体基板の作製方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、半導体基板の作製方法に関する。更に詳しくは、誘電体分離あるいは、絶縁物上の単結晶半導体、半動体基板上の単結晶化合物半導体の作製方法、さらに単結晶半導体層に作成される電子デバイス、集積回路に適する半導体基板の作製方法に関するものである。

【０００２】

【従来の技術】絶縁物上の単結晶Ｓｉ半導体層の形成は、シリコン　オン　インシュレーター（ＳＯＩ）技術として広く知られ、通常のＳｉ集積回路を作製するバルクＳｉ基板では到達しえない数々の優位点をＳＯＩ技術を利用したデバイスが有することから多くの研究が成されてきた。すなわち、ＳＯＩ技術を利用することで、

１．誘電体分離が容易に高集積化が可能、
２．対放射線耐性に優れている、
３．浮遊容量が低減され高速化が可能、

４．ウェル工程が省略できる、

５．ラッチアップを防止できる、

６．薄膜化による完全空乏型電界効果トランジスタが可能、等の優位点が得られる。

【０００３】上記したようなデバイス特性上の多くの利点を実現するために、ここ数十年に渡り、ＳＯＩ構造の形成方法について研究されてきている。この内容は、例えば以下の文献にまとめられている。

【０００４】Ｓｐｅｃｉａｌ　Ｉｓｓｕｅ：“Ｓｉｎｇｌｅ－ｃｒｙｓｔａｌ　ｓｉｌｉｃｏｎ　ｏｎ　ｎｏｎ－ｓｉｎｇｌｅ－ｃｒｙｓｔａｌ　ｉｎｓｕｌａｔｏｒｓ”；ｅｄｉｔｅｄ　ｂｙ　Ｇ．Ｗ．Ｃｕｌｌｅｎ，Ｊｏｕｒｎａｌ　ｏｆ　Ｃｒｙｓｔａｌ　Ｇｒｏｗｔｈ，ｖｏｌｕｍｅ　６３，ｎｏ３，ｐｐ４２９～５９０（１９８３）．また、古くは、単結晶サファイア基板上に、ＳｉをＣＶＤ（化学気相法）で、ヘテロエピタキシーさせて形成するＳＯＳ（シリコン　オン　サファイア）が知られており、最も成熟したＳＯＩ技術として一応の成功は収めはしたが、Ｓｉ層と下地サファイア基板界面の格子不整合により大量の結晶欠陥、サファイア基板からのアルミニュームのＳｉ層への混入、そして何よりも基板の高価格と大面積化への遅れにより、その応用の広がりが妨げられている。比較的近年には、サファイア基板を使用せずにＳＯＩ構造を実現しようという試みが行なわれている。この試みは、次の二つに大別される。

【０００５】１．Ｓｉ単結晶基板を表面酸化後に、窓を開けてＳｉ基板を部分的に表出させ、その部分をシードとして横方向へエピタキシャル成長させ、SiO_2 上へＳｉ単結晶層を形成する。（この場合には、SiO_2 上にＳｉ層の堆積をともなう。）

２．Ｓｉ単結晶基板そのものを活性層として使用し、その下部にSiO_2 を形成する。（この方法は、Ｓｉ層の堆積をともなわない。）また、化合物半導体上のデバイスはＳｉでは得られない高い性能、たとえば、高速、発光など、を持っている。現在は、これらのデバイスはほとんどＧａＡｓ等の化合物半導体基板上にエピタキシャル成長をしてその中に作り込まれている。

【０００６】しかし、化合物半導体基板は、高価で、機械的強度が低く、大面積ウェハは作成が困難などの問題点がある。

【０００７】このようなことから、安価で、機械的強度も高く、大面積ウェハが作製できるＳｉウェハ上に、化合物半導体をヘテロエピタキシャル成長させる試みがなされている。

【０００８】

【発明が解決しようとしている課題】上記１を実現する手段として、ＣＶＤにより、直接、単結晶層Ｓｉを横方向エピタキシャル成長させる方法、非晶質Ｓｉを堆積して、熱処理により固相横方向エピタキシャル成長させる方法、非晶質あるいは、多結晶Ｓｉ層に電子線、レーザ

一光等のエネルギービームを収束して照射し、溶融再結晶により単結晶層をSiO_2 上に成長させる方法、そして、棒状ヒーターにより帯状に溶融領域を走査する方法（Ｚｏｎｅ　Ｍｅｌｔｉｎｇ　Ｒｅｃｒｙｓｔａｌｌｉｚａｔｉｏｎ）が知られている。これらの方法にはそれぞれ一長一短があるが、その制御性、生産性、均一性、品質に多大の問題を残しており、いまだに、工業的に実用化したものはない。たとえば、ＣＶＤ法は平坦薄膜化するには、犠牲酸化が必要となり、固相成長法ではその結晶性が悪い。また、ビームアニール法では、収束ビーム走査による処理時間と、ビームの重なり具合、焦点調整などの制御性に問題がある。このうち、Ｚｏｎｅ　Ｍｅｌｔｉｎｇ　Ｒｅｃｒｙｓｔａｌｌｉｚａｔｉｏｎ法がもっとも成熟しており、比較的大規模な集積回路も試作されてはいるが、依然として、亜粒界等の結晶欠陥は、多数残留しており、少数キャリヤーデバイスを作成するにいたってない。

【０００９】上記２の方法であるＳｉ基板をエピタキシャル成長の種子として用いない方法に於いては、次の４種類の方法が挙げられる。

【００１０】１．Ｖ型の溝が表面に異方性エッチングされたＳｉ単結晶基板に酸化膜を形成し、該酸化膜上に多結晶Ｓｉ層をＳｉ基板と同じ程厚く堆積した後、Ｓｉ基板の裏面から研磨によって、厚い多結晶Ｓｉ層上にＶ溝に囲まれて誘電分離されたＳｉ単結晶領域を形成する。この手法に於ては、結晶性は、良好であるが、多結晶Ｓｉを数百ミクロンも厚く堆積する工程、単結晶Ｓｉ基板を裏面より研磨して分離したＳｉ活性層のみを残す工程に、制御性と生産性の点から問題がある。

【００１１】２．サイモックス（ＳＩＭＯＸ：Ｓｅｐｅｒａｔｉｏｎ　ｂｙ　ｉｏｎ　ｉｍｐｌａｎｔｅｄ　ｏｘｙｇｅｎ）と称されるＳｉ単結晶基板中に酸素のイオン注入によりSiO_2 層を形成する方法であり、Ｓｉプロセスと整合性が良いため現在もっとも成熟した手法である。しかしながら、SiO_2 層を形成するためには、酸素イオンを10^{18} ｉｏｎｓ／ｃｍ^2 以上も注入する必要があるが、その注入時間は長大であり、生産性は高いとはいえず、また、ウェハーコストは高い。更に、結晶欠陥は多く残存し、工業的に見て、少数キャリヤーデバイスを作製できる充分な品質に至っていない。

【００１２】３．多孔質Ｓｉの酸化による誘電体分離によりＳＯＩ構造を形成する方法。この方法は、Ｐ型Ｓｉ単結晶基板表面にＮ型Ｓｉ層をプロトンイオン注入、（イマイ他，Ｊ．Ｃｒｙｓｔａｌ　Ｇｒｏｗｔｈ，ｖｏｌ　６３，５４７（１９８３）），もしくは、エピタキシャル成長とパターニングによって島状に形成し、表面よりＳｉ島を囲むようにＨＦ溶液中の陽極化成法によりＰ型Ｓｉ基板のみを多孔質化したのち、増速酸化によりＮ型Ｓｉ島を誘電体分離する方法である。本方法では、分離されているＳｉ領域は、デバイス工程のまえに決定

されており、デバイス設計の自由度を制限する場合があるという問題点がある。

【００１３】また、上記のような従来のＳＯＩの形成方法とは別に、近年、Ｓｉ単結晶基板を、熱酸化した別のＳｉ単結晶基板に、熱処理又は接着剤を用いて張り合せ、ＳＯＩ構造を形成する方法が注目を浴びている。この方法は、デバイスのための活性層を均一に薄膜化する必要がある。すなわち、数百ミクロンもの厚さのＳｉ単結晶基板をミクロンオーダーかそれ以下に薄膜化する必要がある。この薄膜化には以下のように２種類の方法がある。

【００１４】１．研磨による薄膜化

２．選択エッチングによる薄膜化

１の研磨では均一に薄膜化することが困難である。特にサブミクロンの薄膜化は、ばらつきが数十%にもなってしまい、この均一化は大きな問題となっている。さらにウェハの大口径化が進めばその困難度は増すばかりである。

【００１５】また、２のエッチングは均一な薄膜化に有効とされているが、

・せいぜい10^2と選択比が充分でない

・エッチング後の表面性が悪い

・イオン注入、高濃度Ｂドープ Ｓｉ層上のエピタキシャル成長あるいはヘテロエピタキシャル成長を用いているためＳＯＩ層の結晶性が悪い等の問題点がある（C. Harendt, et. al., J. Elect. Mater. Vol. 20, 267 (1991)、H. Baumgart, et. al., Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp－733 (1991)、C. E. Hunt, Extended Abstract ofECS 1st International Symposium of Wafer Bonding, pp－696 (1991)）。

【００１６】さらに貼り合わせを用いた半導体基板は、必ず２枚のウェハを必要とし、そのうち１枚はほとんど大部分が研磨・エッチング等により無駄に除去され捨てられてしまい、限りある地球の資源を無駄使いしてしまう。

【００１７】したがって、貼り合わせによるＳＯＩにおいては、現状の方法では、その制御性、均一性さらには経済性に多くの問題点が存在する。

【００１８】また、ガラスに代表される光透過性基板上には、一般には、その結晶構造の無秩序性から、堆積した薄膜Ｓｉ層は、基板の無秩序性を反映して、非晶質か、良くて多結晶層にしかならず、高性能なデバイスは作製できない。それは、基板の結晶構造が非晶質であることによっており、単に、Ｓｉ層を堆積しても、良質な単結晶層は得られない。

【００１９】ところで、光透過性基板は、光受光素子であるコンタクトセンサーや投影型液晶画像表示装置を構成するうえにおいて重要である。そして、センサーや表示装置の画素（絵素）をより一層、高密度化、高解像度化、高精密化するには、高性能な駆動素子が必要となる。その結果、光透過性基板上に設けられている素子としても優れた結晶性を有する単結晶層を用いて作製されることが必要となる。

【００２０】したがって、非晶質Ｓｉや多結晶Ｓｉでは、その欠陥の多い結晶構造ゆえに要求されるあるいは今後要求されるに十分な性能を持った駆動素子を作製することが難しい。

【００２１】上で述べたように、化合物半導体のデバイス作製には化合物半導体の基板が必要不可欠となっている。しかし、化合物半導体の基板は高価で、しかも、大面積化が非常に困難である。

【００２２】さらに、Ｓｉ基板上にＧａＡｓ等の化合物半導体をエピタキシャル成長させることが試みられているが、格子定数や熱膨張係数の違いにより、その成長膜は結晶性が悪く、デバイスに応用することは非常に困難となっている。

【００２３】また、格子のミスフィットを緩和するため多孔質Ｓｉ上に化合物半導体をエピタキシャル成長させることが試みられているが、多孔質Ｓｉの熱安定性の低さ、経時変化等によりデバイスを作製中あるいは、作製した後の基板としての安定性、信頼性に欠ける。

【００２４】こうしたなか、本発明の発明者である米原隆夫は、上述した課題点に鑑み、先に特開平５－２１３３８号公報に開示された新規な半導体部材の製造方法を提案した。

【００２５】当該公報に開示された方法は、次のとおりのものである。即ち、多孔質単結晶半導体領域上に非多孔質単結晶半導体領域を配した部材を形成し、前記非多孔質単結晶半導体領域の表面に、表面が絶縁性物質で構成された部材の表面を貼り合わせた後、前記多孔質単結晶半導体領域をエッチングにより除去することを特徴とする半導体部材の製造方法である。

【００２６】当該方法は、上述した課題を解決し得る優れたものである。しかしながら、当該公報に開示された方法を更に発展させて半導体基板の生産性の向上、低コスト化が更に図れれば、当該技術分野に係る産業への寄与は極めて大きなものとなる。

【００２７】［発明の目的］本発明は、上述の公報に開示された方法を、更に改善した半導体基板の作製方法を提供することを目的とする。

【００２８】本発明の別の目的は、経済性に優れて、大面積に渡り均一平坦な、極めて優れた結晶性を有する単結晶基板を用いて、表面に形成された半導体層あるいは化合物半導体活性層を残して、その片面から該活性層までを取り去り、絶縁物上に欠陥の著しく少ない単結晶層

あるいは化合物半導体結晶層を得る半導体基板の作製方法を提供することにある。

【００２９】本発明の更に別の目的は、透明基板（光透過性基板）上に結晶性が単結晶ウェハー並に優れたＳｉあるいは化合物半導体単結晶層を得るうえで、生産性、均一性、制御性、コストの面において卓越した半導体基板の作製方法を提案することにある。

【００３０】本発明の更に別の目的は、ＳＯＩ構造の大規模集積回路を作製する際にも、高価なＳＯＳや、ＳＩＭＯＸの代替足り得る半導体基板の作製方法を提案することにある。

【００３１】

【課題を解決するための手段】本発明の半導体基板の作製方法は、下述する構成のものである。

【００３２】即ち、本発明の半導体基板の作製方法の第１の態様は、多孔質層を有する第１の基体の前記多孔質層上に非多孔質単結晶半導体層を形成する工程、前記非多孔質単結晶半導体層を第２の基体と貼り合わせる工程、前記貼り合わせて構成された基体を前記多孔質層において分離する工程、前記分離された第２の基体上に配された多孔質層を除去する工程、及び前記分離された第１の基体を構成する多孔質層を除去する工程を有することを特徴とするものである。

【００３３】本発明の第２の態様は、多孔質層を有する第１の基体の前記多孔質層上に非多孔質単結晶半導体層を形成する工程、前記非多孔質単結晶半導体層を第２の基体と絶縁層を介して貼り合わせる工程、前記貼り合わせて構成された基体を前記多孔質層において分離する工程、前記分離された第２の基体上に配された多孔質層を除去する工程、及び前記分離された第１の基体を構成する多孔質層を除去する工程を有することを特徴とするものである。

【００３４】

【作用】本発明においては、貼り合わせて構成された基体を多孔質層で分離し、非多孔質単結晶半導体層が配された第２の基体上の多孔質層を除去することにより、高品質な非多孔質単結晶半導体層が配された半導体基体を形成できる。これに加えて、貼り合わせて構成された基体を多孔質層で分離し、第１の基体を構成する多孔質層を除去することにより、多孔質層を除去した第１の基体を半導体基体作製に再利用することができる。これにより、半導体基体の生産性の向上、低コスト化が更に図れる。

【００３５】本発明によれば、透明基板（光透過性基板）をはじめとする基板上に結晶性が単結晶ウェハー並に優れたＳｉ等の単結晶層あるいは化合物半導体単結晶層を得るうえで、生産性、均一性、制御性、コストの面において卓越した半導体基板の作製方法を提案することができる。

【００３６】また、本発明によれば、ＳＯＩ構造の大規模集積回路を作製する際にも、高価なＳＯＳや、ＳＩＭＯＸの代替足り得る半導体基板の作製方法を提案することができる。

【００３７】本発明においては、多孔質層を介して基体を２つ以上に分離することができ、分離後の一方の基体は、残留多孔質を除去した後、半導体基板として使用可能であり、他方の基体は、残留多孔質を除去した後、再度、半導体基板の作製に利用することができる。

【００３８】本発明においては、基体の両面に多孔質層および非多孔質単結晶層を形成し、該単結晶層を挟むように２枚の別の基体を貼り合わせた後、前記多孔質層で基体を分離することにより同時に２枚の半導体基板を作製することができる。

【００３９】本発明の半導体基板の作製方法をシリコンを例に挙げて以下に詳細に説明する。

【００４０】多孔質Ｓｉの機械的強度はｐｏｒｏｓｉｔｙにより異なるが、バルクＳｉよりも十分に弱いと考えられる。たとえば、ｐｏｒｏｓｉｔｙが５０％であれば機械的強度はバルクの半分と考えて良い。すなわち、貼り合わせウェハに圧縮、引っ張りあるいは剪断力をかけると、まず多孔質Ｓｉ層が破壊されることになる。また、ｐｏｒｏｓｉｔｙを増加させればより弱い力で多孔質層を破壊できる。

【００４１】Ｓｉ基板はＨＦ溶液を用いた陽極化成法によって多孔質化させることができる。この多孔質Ｓｉ層は、単結晶Ｓｉの密度２．３３ｇ／ｃｍ^3 に比べて、ＨＦ溶液濃度を５０～２０％に変化させることでその密度を１．１～０．６ｇ／ｃｍ^{3}の範囲に変化させることができる。この多孔質層は、下記の理由により、Ｎ型Ｓｉ層には形成されず、Ｐ型Ｓｉ基板のみに形成される。この多孔質Ｓｉ層は、透過電子顕微鏡による観察によれば、平均約６００オングストローム程度の径の孔が形成される。

【００４２】多孔質Ｓｉは、Ｕｈｌｉｒ等によって１９５６年に半導体の電解研磨の研究過程において発見された（A. Uhlir, Bell Syst. Tech. J., vol. 35, 333 (1956)）。

【００４３】また、ウナガミ等は陽極化成におけるＳｉの溶解反応を研究し、ＨＦ溶液中のＳｉの陽極反応には正孔が必要であり、その反応は、次のようであると報告している（T. ウナガミ、J. Electrochem. Soc., vol. 127, 476 (1980)）。

【００４４】$Si+2HF+(2-n)e^+ \rightarrow SiF_2+2H^+ +ne^-$

$SiF_2+2HF \rightarrow SiF_4+H_2$

$SiF_4+2HF \rightarrow H_2SiF_6$

または、

$Si+4HF+(4-\lambda)e^+ \rightarrow SiF_4+4H^+ +\lambda e^-$

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$SiF_4 + 2HF \rightarrow H_2 SiF_6$

ここで、e^+およびe^-はそれぞれ正孔と電子を表している。また、nおよびλはそれぞれＳｉ原子が溶解するために必要な正孔の数であり、ｎ＞２またはλ＞４なる条件が満たされる場合に多孔質Ｓｉが形成されるとしている。

【００４５】以上のことから、正孔の存在するＰ型Ｓｉは多孔質化されるが、Ｎ型Ｓｉは多孔質化されない。この多孔質化における選択性は長野等および今井によって実証されている（長野、中島、安野、大中、梶原、電子通信学会技術研究報告、ｖｏｌ．７９，ＳＳＤ７９－９５４９（１９７９））、（Ｋ．Ｉｍａｉ，Ｓｏｌｉｄ－Ｓｔａｔｅ Ｅｌｅｃｔｒｏｎｉｃｓ，ｖｏｌ．２４，１５９（１９８１））。

【００４６】しかし、高濃度Ｎ型Ｓｉであれば多孔質化されるとの報告もあり（Ｒ．Ｐ．Ｈｏｌｍｓｔｒｏｍ ａｎｄ Ｊ．Ｙ．Ｃｈｉ，Ａｐｐｌ．Ｐｈｙｓ．Ｌｅｔｔ．，ｖｏｌ．４２，３８６（１９８３））、Ｐ型、Ｎ型の別にこだわらず、多孔質化を実現できる基板を選ぶことが重要である。

【００４７】多孔質Ｓｉ層には、透過電子顕微鏡による観察によれば、平均約６００オングストローム程度の径の孔が形成されており、その密度は単結晶Ｓｉに比べると、半分以下になるにもかかわらず、単結晶性は維持されており、多孔質層の上部へ単結晶Ｓｉ層をエピタキシャル成長させることも可能である。ただし、１０００℃以上では、内部の孔の再配列が起こり、増速エッチングの特性が損なわれる。このため、Ｓｉ層のエピタキシャル成長には、分子線エピタキシャル成長、プラズマＣＶＤ、減圧ＣＶＤ法、光ＣＶＤ、バイアス・スパッター法、液相成長法等の低温成長が好適とされている。

【００４８】また、多孔質層はその内部に大量の空隙が形成されている為に、密度が半分以下に減少する。その結果、体積に比べて表面積が飛躍的に増大するため、その化学エッチング速度は、通常の単結晶層のエッチング速度に比べて、著しく増速される。

【００４９】［実施態様例１］図１（ａ）に示すように、まず第１のＳｉ単結晶基板１１を用意して、その表面層を多孔質化１２し、多孔質Ｓｉ１２上に非多孔質単結晶Ｓｉ層１３を形成する（図１（ｂ））。

【００５０】次に、図１（ｃ）に示すように、もう一方のＳｉ支持基板１４と単結晶Ｓｉ層１３とを絶縁層１５を介して室温で密着させた後、陽極接合、加圧、あるいは熱処理、あるいはこれらの組み合わせにより貼り合わせる。これにより、Ｓｉ支持基板１４と単結晶層１３とは絶縁層１５を介して強固に結合する。絶縁層１５は単結晶Ｓｉ層上、Ｓｉ支持基板１４上の少なくとも一方に形成する、あるいは絶縁性の薄板をはさみ３枚重ねで貼り合わせる。

【００５１】次に、多孔質Ｓｉ層１２で基板を分離する

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（図１（ｄ））。Ｓｉ支持基板側は、多孔質Ｓｉ１２／単結晶Ｓｉ層１３／絶縁層１５／Ｓｉ支持基板１４のような構造となる。

【００５２】さらに、多孔質Ｓｉ１２を選択的に除去する。通常のＳｉのエッチング液、あるいは多孔質Ｓｉの選択エッチング液である弗酸、あるいは弗酸にアルコールおよび過酸化水素水の少なくともどちらか一方を添加した混合液、あるいは、バッファード弗酸あるいはバッファード弗酸にアルコールおよび過酸化水素水の少なくともどちらか一方を添加した混合液の少なくとも１種類を用いて、多孔質Ｓｉ１２のみを無電解湿式化学エッチングして絶縁性基板１５＋１４上に薄膜化した単結晶Ｓｉ層１３を残存させ形成する。上記詳述したように、多孔質Ｓｉの膨大な表面積により通常のＳｉのエッチング液でも選択的に多孔質Ｓｉのみをエッチングすることが可能である。

【００５３】あるいは、単結晶Ｓｉ層１３を研磨ストッパーとして多孔質Ｓｉ１２を選択研磨で除去する。

【００５４】図１（ｅ）には、本発明で得られる半導体基板が示される。絶縁性基板１５＋１４上に単結晶Ｓｉ層１３が平坦に、しかも均一に薄層化されて、ウェハ全域に、大面積に形成される、こうして得られた半導体基板は、絶縁分離された電子素子作製という点から見ても好適に使用することができる。

【００５５】第１のＳｉ単結晶基板１１は、残留多孔質Ｓｉを除去して、表面平坦性が許容できないほど荒れている場合には、表面平坦化を行なった後、再度第１のＳｉ単結晶基板１１として使用する。

【００５６】本発明において、多孔質Ｓｉ層で２つの基体を分離する方法としては、貼り合わせた基体の両側より加圧して多孔質層を押しつぶす方法、それぞれの基体を両側に引き、両者を分離する方法、多孔質層に治具をそう入する方法、貼り合わせた基体の表面に平行な方向に力を加える方法、多孔層に超音波振動を加える方法等が採用できる。

【００５７】本発明において、分離に適した多孔質Ｓｉ層の多孔度（ｐｏｒｏｓｉｔｙ）は、一般的には１０～８０％の範囲であり、より好ましくは、２０～６０％の範囲である。

【００５８】［実施態様例２］図２（ａ）に示すように、まず第１のＳｉ単結晶基板２１を用意して、その表面層を多孔質化２２し、多孔質Ｓｉ２２上に非多孔質単結晶Ｓｉ層２３を形成する（図２（ｂ））。

【００５９】次に、図２（ｃ）に示すように、石英やガラスに代表される光透過性支持基板２４と単結晶Ｓｉ層２３とを絶縁層２５を介して室温で密着させた後、陽極接合、加圧、あるいは熱処理、あるいはこれらの組み合わせにより貼り合わせる。これにより、光透過性支持基板２４と単結晶層２３とは絶縁層２５を介して強固に結合する。絶縁層２５は単結晶Ｓｉ層上、光透過性支持基

板２４上の少なくとも一方に形成する、あるいは絶縁性の薄板をはさみ３枚重ねで貼り合わせる。

【００６０】次に、多孔質Ｓｉ層２３で基板を分割する（図２（ｄ））。光透過性支持基板側は、多孔質Ｓｉ２２／単結晶Ｓｉ層２３／絶縁層２５／光透過性支持基板２４のような構造となる。

【００６１】さらに、多孔質Ｓｉ２２を選択的に除去する。通常のＳｉのエッチング液、あるいは多孔質Ｓｉの選択エッチング液である弗酸、あるいは弗酸にアルコールおよび過酸化水素水の少なくともどちらか一方を添加した混合液、あるいは、バッファード弗酸あるいはバッファード弗酸にアルコールおよび過酸化水素水の少なくともどちらか一方を添加した混合液の少なくとも１種類を用いて、多孔質Ｓｉ２２のみを無電解湿式化学エッチングして光透過性絶縁性基板２５＋２４上に薄膜化した単結晶Ｓｉ層２３を残存させ形成する。上記詳述したように、多孔質Ｓｉの膨大な表面積により通常のＳｉのエッチング液でも選択的に多孔質Ｓｉのみをエッチングすることが可能である。

【００６２】あるいは、単結晶Ｓｉ層２３を研磨ストッパーとして多孔質Ｓｉ２２を選別研磨で除去する。

【００６３】図２（ｅ）には、本発明で得られる半導体基板が示される。光透過性絶縁性基体２５＋２４上に単結晶Ｓｉ層２３が平坦に、しかも均一に薄層化されて、ウェハ全域に、大面積に形成される。こうして得られた半導体基板は、絶縁分離された電子素子作製という点から見ても好適に使用することができる。

【００６４】絶縁介在層２５はなくても良い。

【００６５】第１のＳｉ単結晶基板２１は、残留多孔質Ｓｉを除去して、表面平坦性が許容できないほど荒れている場合には、表面平坦化を行なった後、再度第１のＳｉ単結晶基板２１として使用できる。

【００６６】［実施態様例３］図３（ａ）に示すように、まず第１のＳｉ単結晶基板３１を用意して、その表面層を多孔質化３２し、多孔質Ｓｉ３２上に非多孔質単結晶化合物半導体層３３を形成する（図３（ｂ））。

【００６７】次に、図３（ｃ）に示すように、もう一方のＳｉ支持基板３４と単結晶化合物半導体層３３とを絶縁層３５を介して室温で密着させた後、陽極接合、加圧、あるいは熱処理、あるいはこれらの組み合わせにより貼り合わせる。これにより、Ｓｉ支持基板３４と単結晶層３３とは絶縁層３５を介して強固に結合する。絶縁層３５は単結晶化合物半導体層上、Ｓｉ支持基板３４上の少なくとも一方に形成する、あるいは絶縁性の薄板をはさみ３枚重ねて貼り合わせる。

【００６８】次に、多孔質Ｓｉ層３２で基板を分割する（図３（ｄ））。Ｓｉ支持基板側は、多孔質Ｓｉ３２／単結晶化合物半導体層３３／絶縁層３５／Ｓｉ支持基板３４のような構造となる。

【００６９】さらに、多孔質Ｓｉ３２を選択的に除去する。化合物半導体に対してＳｉのエッチング速度の早いエッチング液を用いて、多孔質Ｓｉ３２のみを化学エッチングして絶縁性基板３５＋３４上に薄膜化した単結晶化合物半導体層３３を残存させ形成する。

【００７０】あるいは、単結晶化合物半導体層３３を研磨ストッパーとして多孔質Ｓｉ３２を選択研磨で除去する。

【００７１】図３（ｅ）には、本発明で得られる半導体基板が示される。絶縁性基板３５＋３４上に単結晶化合物半導体層３３が平坦に、しかも均一に薄層化されて、ウェハ全域に、大面積に形成される。こうして得られた半導体基板は、化合物半導体基板として、さらには絶縁分離された電子素子作製という点から見ても好適に使用することができる。

【００７２】化合物半導体基板として用いる場合には絶縁層３５はなくても良い。

【００７３】第１のＳｉ単結晶基板３１は、残留多孔質Ｓｉを除去して、表面平坦性が許容できないほど荒れている場合には、表面平坦化を行なった後、再度第１のＳｉ単結晶基板３１として使用できる。

【００７４】［実施態様例４］図４（ａ）に示すように、まず第１のＳｉ単結晶基板４１を用意して、その表面層を多孔質化４２し、多孔質Ｓｉ４２上に非多孔質単結晶化合物半導体層４３を形成する（図４（ｂ））。

【００７５】次に、図４（ｃ）に示すように、石英やガラスに代表される光透過性支持基板４４と単結晶化合物半導体層４３とを絶縁層４５を介して室温で密着させた後、陽極接合、加圧、あるいは熱処理、あるいはこれらの組み合わせにより貼り合わせる。これにより、光透過性支持基板４４と単結晶層４３とは絶縁層４５を介して強固に結合する。絶縁層４５は単結晶化合物半導体層上、光透過性支持基板４４上の少なくとも一方に形成する、あるいは絶縁性の薄板をはさみ３枚重ねで貼り合わせる。

【００７６】次に、多孔質Ｓｉ層４３で基板を分割する（図４（ｄ））。光透過性支持基板側は、多孔質Ｓｉ４２／単結晶化合物半導体層４３／絶縁層４５／光透過性支持基板４４のような構造となる。

【００７７】さらに、多孔質Ｓｉ４２を選択的に除去する。化合物半導体に対してＳｉのエッチング速度の速いエッチング液を用いて、多孔質Ｓｉ４２のみを化学エッチングして絶縁性基板４５＋４４上に薄膜化した単結晶化合物半導体層４３を残存させ形成する。

【００７８】あるいは、単結晶化合物半導体層４３を研磨ストッパーとして多孔質Ｓｉ４２を選択研磨で除去する。

【００７９】図４（ｅ）には、本発明で得られる半導体基板が示される。光透過性絶縁性基板４５＋４４上に単結晶化合物半導体層４３が平坦に、しかも均一に薄層化されて、ウェハ全域に、大面積に形成される。こうして

得られた半導体基板は、絶縁分離された電子素子作製という点から見ても好適に使用することができる。

【００８０】絶縁介在層４５はなくても良い。

【００８１】第１のＳｉ単結晶基板４１は、残留多孔質Ｓｉを除去して、表面平坦性が許容できないほど荒れている場合には、表面平坦化を行なった後、再度第１のＳｉ単結晶基板４１として使用できる。

【００８２】［実施態様例５］図５（ａ）に示すように、まず第１のＳｉ単結晶基板５１を用意して、その両面の表面層を多孔質化５２、５３し、両面の多孔質Ｓｉ５２、５３上に非多孔質単結晶半導体層５４、５５を形成する（図５（ｂ））。

【００８３】次に、図５（ｃ）に示すように、２枚の支持基板５６、５７と単結晶半導体層５４、５５とをそれぞれ絶縁層５８、５９を介して室温で密着させた後、陽極接合、加圧、あるいは熱処理、あるいはこれらの組み合わせにより貼り合わせる。これにより、支持基板５６、５７と単結晶層５４、５５とは絶縁層５８、５９を介して強固に結合する。絶縁層５８、５９は単結晶半導体層５４、５５上、支持基板５６、６７上の少なくとも一方に形成する、あるいは絶縁性の薄板をはさみ５枚重ねで貼り合わせる。

【００８４】次に、両多孔質Ｓｉ層５２、５３で基板を三分割する（図５（ｄ））。２枚の支持基板は、多孔質Ｓｉ／単結晶半導体層／絶縁層／支持基板（５２／５４／５８／５６、および５３／５５／５９／５７）のような構造となる。

【００８５】さらに、両多孔質Ｓｉ５２、５３を選択的に除去する。多孔質Ｓｉ５２、５３のみを選択的に化学エッチングして支持基板５８／５６および５９／５７上に薄膜化した単結晶半導体層５４、５５を残存させ形成する。

【００８６】あるいは、単結晶半導体層５４、５５を研磨ストッパーとして多孔質Ｓｉ５２、５３を選択、研磨で除去する。

【００８７】図５（ｅ）には、本発明で得られる半導体基板が示される。支持基板上に単結晶化合物半導体層が平坦に、しかも均一に薄層化されて、ウェハ全域に、大面積に２体同時に形成される。こうして得られた半導体基板は、絶縁分離された電子素子作製という点から見ても好適に使用することができる。

【００８８】絶縁介在層５８、５９はなくても良い。

【００８９】支持基板５６、５７は同一でなくても良い。

【００９０】第１のＳｉ単結晶基板５１は、残留多孔質Ｓｉを除去して、表面平坦性が許容できないほど荒れている場合には、表面平坦化を行なった後、再度第１のＳｉ単結晶５１として使用できる。

【００９１】

【実施例】

（実施例１）６２５μｍの厚みを持った比抵抗０．０１Ω・ｃｍのＰ型の６インチ径の第１の（１００）単結晶Ｓｉ基板を、ＨＦ溶液中において陽極化成を行った。

【００９２】陽極化成条件は以下のとおりであった。

【００９３】電流密度：５（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 1 : 1$

時間：１２（分）

多孔質Ｓｉの厚み：１０（μｍ）

Ｐｏｒｏｓｉｔｙ：１５（％）

この基板を酸素雰囲気中４００℃で１時間酸化した。この酸化により多孔質Ｓｉの孔の内壁は熱酸化膜で覆われた。多孔質Ｓｉ上にＣＶＤ（ＣｈｅｍｉｃａｌＶａｐｏｒ　Ｄｅｐｏｓｉｔｉｏｎ）法により単結晶Ｓｉを１μｍエピタキシャル成長した。成長条件は以下の通りである。

【００９４】ソースガス：SiH_2Cl_2/H_2

ガス流量：０．５／１８０　ｌ／ｍｉｎ

ガス圧力：８０Ｔｏｒｒ

温度：９５０℃

成長速度：０．３μｍ／ｍｉｎ

さらに、このエピタキシャルＳｉ層表面に熱酸化により１００ｎｍのSiO_2層を形成した。

【００９５】該SiO_2層表面と別に用意した５００ｎｍのSiO_2層を形成したＳｉ基板の表面とを重ね合わせ、接触させた後、９００℃－２時間の熱処理をし、貼り合わせをおこなった。

【００９６】貼り合わせたウェハの面に対して垂直方向に均一に十分な引っ張り力を加えたところ多孔質Ｓｉ層が破壊しウェハは二分割され、多孔質Ｓｉが表出した。具体的には、貼り合わせたウェハの両面にプレートを接着剤を用いて接着し、該プレートを該プレートを互いに引き離す方向に移動せしめる治具に配した後、２つに引き離した。

【００９７】その後、多孔質Ｓｉ層を４９％弗酸と３０％過酸化水素水との混合液（１：５）で撹拌しながら選択エッチングした。単結晶Ｓｉはエッチングされずに残り、単結晶Ｓｉをエッチ・ストップの材料として、多孔質Ｓｉは選択エッチングされ、完全に除去された。

【００９８】非多孔質Ｓｉ単結晶の該エッチング液に対するエッチング速度は、極めて低く、多孔質層のエッチング速度との選択比は十の五乗以上にも達し、非多孔質層におけるエッチング量（数十オングストローム程度）は実用上無視できる膜厚減少である。

【００９９】すなわち、Ｓｉ酸化膜上に１μｍの厚みを持った単結晶Ｓｉ層が形成できた。多孔質Ｓｉの選択エッチングによっても単結晶Ｓｉ層には何ら変化はなかった。

【０１００】透過電子顕微鏡による断面観察の結果、Ｓｉ層には新たな結晶欠陥は導入されておらず、良好な結

晶性が維持されていることが確認された。

【０１０１】こうして、高品質な半導体層を有するＳＯＩ基板が得られた。更に、多孔質Ｓｉ層を境に分離した他方のＳｉ基板に残存する多孔質層を同様のエッチングにより除去した後、表面をポリッシングした。こうして得られたＳｉ基板を用いて上述の工程を繰り返すことにより高品質な半導体層を有するＳＯＩ基板複数個が得られた。

【０１０２】（実施例２）５２５μｍの厚みを持った比抵抗０．０１Ω・ｃｍのｐ型の４インチ径の第１の（１００）単結晶Ｓｉ基板を、ＨＦ溶液中において陽極化成を行った。

【０１０３】陽極化成条件は以下のとおりであった。

【０１０４】電流密度：７（ｍＡ・ｃｍ$^{-2}$）

陽極化成溶液：ＨＦ：H_2 Ｏ：C_2 H_5 ＯＨ＝１：１：１

時間：１２（分）

多孔質Ｓｉの厚み：１０（μｍ）

Ｐｏｒｏｓｉｔｙ：１５（％）

この基板を酸素雰囲気中４００℃で２時間酸化した。この酸化により多孔質Ｓｉの孔の内壁は熱酸化膜で覆われた。多孔質Ｓｉ上にＭＢＥ（Ｍｏｌｅｃｕｌａｒ Ｂｅａｍ Ｅｐｉｔａｘｙ）法により単結晶Ｓｉを０．５μｍエピタキシャル成長した。成長条件は以下の通りである。

【０１０５】温度：７００℃

圧力：１×１０$^{-9}$Ｔｏｒｒ

成長速度：０．１ｎｍ／ｓｅｃ

温度：９５０℃

成長速度：０．３μｍ／ｍｉｎ

さらに、このエピタキシャルＳｉ層表面に熱酸化により１００ｎｍのSiO_2層を形成した。

【０１０６】該SiO_2層表面と別に用意した溶融石英基板の表面とを重ね合わせ、接触させた後、４００℃－２時間の熱処理をし、貼り合わせをおこなった。

【０１０７】貼り合わせたウェハの面に対して垂直方向に均一に十分な圧力を加えたところ多孔質Ｓｉ層が破壊しウェハは二分割され、多孔質Ｓｉが表出した。具体的には、貼り合わせたウェハの両面にプレートを接着剤を用いて接着し、該プレートを該プレートを実施例１で述べた治具に配した後、該プレートに圧力を加えることでＳｉ層を破壊した。

【０１０８】その後、多孔質Ｓｉ層をバッファード弗酸と３０％過酸化水素水との混合液（１：５）で撹拌しながら選択エッチングする。単結晶Ｓｉはエッチングされずに残り、単結晶Ｓｉをエッチ・ストップの材料として、多孔質Ｓｉは選択エッチングされ、完全に除去された。

【０１０９】非多孔質Ｓｉ単結晶の該エッチング液に対するエッチング速度は、極めて低く、多孔質層のエッチング速度との選択比は十の五乗以上にも達し、非多孔質層におけるエッチング量（数十オングストローム程度）は実用上無視できる膜厚減少である。

【０１１０】すなわち、溶融石英基板上に０．５μｍの厚みを持った単結晶Ｓｉ層が形成できた。多孔質Ｓｉの選択エッチングによっても単結晶Ｓｉ層には何ら変化はなかった。

【０１１１】透過電子顕微鏡による断面観察の結果、Ｓｉ層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【０１１２】実施例１と同様にして、上述の工程を繰り返すことにより高品質な半導体層を有するＳＯＩ基板複数個が得られた。

【０１１３】（実施例３）６２５μｍの厚みを持った比抵抗０．０１Ω・ｃｍのＰ型あるいはＮ型の６インチ径の第１の（１００）単結晶Ｓｉ基板を、ＨＦ溶液中において陽極化成を行った。

【０１１４】陽極化成条件は以下のとおりであった。

【０１１５】電流密度：７（ｍＡ・ｃｍ$^{-2}$）

陽極化成溶液：ＨＦ：H_2 Ｏ：C_2 H_5 ＯＨ＝１：１：１

時間：１２（分）

多孔質Ｓｉの厚み：１０（μｍ）

Ｐｏｒｏｓｉｔｙ：１５（％）

この基板を酸素雰囲気中４００℃で１時間酸化した。この酸化により多孔質Ｓｉの孔の内壁は熱酸化膜で覆われた。多孔質Ｓｉ上にＭＯＣＶＤ（ＭｅｔａｌＯｒｇａｎｉｃ Ｃｈｅｍｉｃａｌ Ｖａｐｏｒ Ｄｅｐｏｓｉｔｉｏｎ）法により単結晶ＧａＡｓを１μｍエピタキシャル成長した。成長条件は以下の通りである。

【０１１６】ソースガス：ＴＭＧ／AsH_3／H_2

ガス圧力：８０Ｔｏｒｒ

温度：７００℃

該ＧａＡｓ層表面と別に用意した第２のＳｉ基板の表面とを重ね合わせ、接触させた後、９００℃－１時間の熱処理をし、貼り合わせをおこなった。この熱処理により両基板は強固に貼り合わされた。

【０１１７】貼り合わせたウェハに実施例２と同様にして圧力を加えたところ多孔質Ｓｉ層が破壊しウェハは二分割され、多孔質Ｓｉが表出した。

【０１１８】その後、多孔質Ｓｉ層を内壁の酸化膜を弗酸で除去した後、多孔質Ｓｉをエチレンジアミン＋ピロカテコール＋水（１７ｍｌ：３ｇ：８ｍｌの比率）１１０℃でエッチングした。単結晶ＧａＡｓはエッチングされずに残り、単結晶ＧａＡｓをエッチ・ストップの材料として、多孔質Ｓｉは選択エッチングされ、完全に除去された。

【０１１９】単結晶ＧａＡｓの該エッチング液に対するエッチング速度は、極めて低く、実用上無視できる膜厚減少である。

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【０１２０】すなわち、Ｓｉ基板上に１μｍの厚みを持った単結晶ＧａＡｓ層が形成できた。多孔質Ｓｉの選択エッチングによっても単結晶ＧａＡｓ層には何ら変化はなかった。

【０１２１】透過電子顕微鏡による断面観察の結果、ＧａＡｓ層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【０１２２】実施例２と同様にして、上述の工程を繰り返し、高品質なＧａＡｓ層を配した複数の半導体基板が得られた。

【０１２３】支持基板として酸化膜付きのＳｉ基板を用いることにより、絶縁膜上のＧａＡｓも同様に作製できた。

【０１２４】（実施例４）６２５μｍの厚みを持った比抵抗０．０１Ω・ｃｍのｐ型あるいはＮ型の５インチ径の第１の（１００）単結晶Ｓｉ基板を、ＨＦ溶液中において陽極化成を行った。

【０１２５】陽極化成条件は以下のとおりであった。

【０１２６】電流密度：１０（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 1 : 1$

時間：２４（分）

多孔質Ｓｉの厚み：２０（μｍ）

Ｐｏｒｏｓｉｔｙ：１７（％）

この基板を酸素雰囲気中４００℃で２時間酸化した。この酸化により多孔質Ｓｉの孔の内壁は熱酸化膜で覆われた。多孔質Ｓｉ上にＭＢＥ（Ｍｏｌｅｃｕｌａｒ　Ｂｅａｍ　Ｅｐｉｔａｘｙ）法により単結晶ＡｌＧａＡｓを０．５μｍエピタキシャル成長した。

【０１２７】該ＡｌＧａＡｓ層表面と別に用意した低融点ガラス基板の表面とを重ね合わせ、接触させた後、５００℃－２時間の熱処理をし、貼り合わせをおこなった。この熱処理により両基板は強固に貼り合わされた。

【０１２８】貼り合わせたウェハ実施例２と同様にして圧力を加えたところ多孔質Ｓｉ層が破壊しウェハは二分割され、多孔質Ｓｉが表出した。

【０１２９】その後、多孔質Ｓｉを弗酸溶液でエッチングした。単結晶ＡｌＧａＡｓはエッチングされずに残り、単結晶ＡｌＧａＡｓをエッチ・ストップの材料として、多孔質Ｓｉは選択エッチングされ、完全に除去された。

【０１３０】単結晶ＡｌＧａＡｓの該エッチング液に対するエッチング速度は、極めて低く、実用上無視できる膜厚減少である。

【０１３１】すなわち、ガラス基板上に０．５μｍの厚みを持った単結晶ＡｌＧａＡｓ層が形成できた。多孔質Ｓｉの選択エッチングによっても単結晶ＡｌＧａＡｓ層には何ら変化はなかった。

【０１３２】透過電子顕微鏡による断面観察の結果、ＡｌＧａＡｓ層には新たな結晶欠陥は導入されておらず、

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良好な結晶性が維持されていることが確認された。実施例２と同様にして、上述の工程を繰り返すことにより高品質な半導体層を有する基板が複数個得られた。

【０１３３】（実施例５）６２５μｍの厚みを持った比抵抗０．０１Ω・ｃｍのｐ型あるいはＮ型の両面研磨の６インチ径の第１の（１００）単結晶Ｓｉ基板を、ＨＦ溶液中において両面に対して陽極化成を行った。

【０１３４】陽極化成条件は以下のとおりであった。

【０１３５】電流密度：５（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 1 : 1$

時間：１２×２（分）

多孔質Ｓｉの厚み：各１０（μｍ）

Ｐｏｒｏｓｉｔｙ：１５（％）

この基板を酸素雰囲気中４００℃で１時間酸化した。この酸化により多孔質Ｓｉの孔の内壁は熱酸化膜で覆われた。両面に形成した多孔質Ｓｉ上にＣＶＤ（Ｃｈｅｍｉｃａｌ　Ｖａｐｏｒ　Ｄｅｐｏｓｉｔｉｏｎ）法により単結晶Ｓｉをそれぞれ１μｍエピタキシャル成長した。成長条件は以下の通りである。

【０１３６】ソースガス：SiH_2Cl_2/H_2

ガス流量：０．５／１８０　ｌ／ｍｉｎ

ガス圧力：８０Ｔｏｒｒ

温度：９５０℃

成長速度：０．３μｍ／ｍｉｎ

さらに、このエピタキシャルＳｉ層表面に熱酸化により１００ｎｍのSiO_2層を形成した。

【０１３７】該SiO_2層表面と別に用意した５００ｎｍのSiO_2層を形成した２枚のＳｉ基板の表面とをそれぞれ重ね合わせ、接触させた後、６００℃－２時間の熱処理をし、貼り合わせをおこなった。

【０１３８】実施例１の手法を用いて貼り合わせたウェハの面に対して垂直方向に十分な引っ張り力を加えたところ多孔質Ｓｉ層が２層とも破壊しウェハは三分割され、多孔質Ｓｉが表出した。

【０１３９】その後、多孔質Ｓｉ層を４９％弗酸と３０％過酸化水素水との混合液（１：５）で撹拌しながら選択エッチングする。単結晶Ｓｉはエッチングされずに残り、単結晶Ｓｉをエッチ・ストップの材料として、多孔質Ｓｉは選択エッチングされ、完全に除去された。

【０１４０】非多孔質Ｓｉ単結晶の該エッチング液に対するエッチング速度は、極めて低く、多孔質層のエッチング速度との選択比は十の五乗以上にも達し、比多孔質層におけるエッチング量（数十オングストローム程度）は実用上無視できる膜厚減少である。

【０１４１】すなわち、Ｓｉ酸化膜上に１μｍの厚みを持った単結晶Ｓｉ層が２枚同時に形成できた。多孔質Ｓｉの選択エッチングによっても単結晶Ｓｉ層には何ら変化はなかった。

【０１４２】透過電子顕微鏡による断面観察の結果、Ｓ

ｉ層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。実施例１と同様にして上述の工程を繰り返し、高品質な半導体層を有する基板複数個を得た。

【０１４３】（実施例６）６２５μｍの厚みを持った比抵抗０．０１Ω・ｃｍのＰ型あるいはＮ型の５インチ径の第１の（１００）単結晶Ｓｉ基板を、ＨＦ溶液中において陽極化成を行った。

【０１４４】陽極化成条件は以下のとおりであった。

【０１４５】電流密度：７（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 1 : 1$

時間：４（分）

多孔質Ｓｉの厚み：３（μｍ）

Ｐｏｒｏｓｉｔｙ：１５（％）

さらに

電流密度：３０（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 3 : 2$

時間：３（分）

多孔質Ｓｉの厚み：１０（μｍ）

Ｐｏｒｏｓｉｔｙ：４５（％）

この基板を酸素雰囲気中４００℃で１時間酸化した。この酸化により多孔質Ｓｉの孔の内壁は熱酸化膜で覆われた。多孔質Ｓｉ上にＣＶＤ法により単結晶Ｓｉを０．３μｍエピタキシャル成長した。成長条件は以下の通りである。

【０１４６】ソースガス：SiH_4

キャリヤーガス：H_2

温度：８５０℃

圧力：1×10^{-2}Ｔｏｒｒ

成長速度：３．３ｎｍ／ｓｅｃ

さらに、このエピタキシャルＳｉ層表面に熱酸化により１００ｎｍのＳｉO_2層を形成した。

【０１４７】該ＳｉO_2層表面と別に用意した５００ｎｍのＳｉO_2層を形成したＳｉ基板の表面とを重ね合わせ、接触させた後、７００℃－２時間の熱処理をし、貼り合わせをおこなった。

【０１４８】実施例１の手法を用いて、貼り合わせたウェハの面に対して垂直方向に十分な引っ張り力を加えたところで多孔質Ｓｉ層が破壊しウェハは二分割され、多孔質Ｓｉが表出した。

【０１４９】その後、多孔質Ｓｉ層を$HF/HNO_3/CH_3COOH$系のエッチング液で選択エッチングする。多孔質Ｓｉはエッチングされ、完全に除去された。

【０１５０】非多孔質Ｓｉ単結晶の該エッチング液に対するエッチング速度は、極めて低く、非多孔質層におけるエッチング量は実用上無視できる膜厚減少である。

【０１５１】すなわち、Ｓｉ酸化膜上に１μｍの厚みを持った単結晶Ｓｉ層が形成できた。多孔質Ｓｉの選択エッチングによっても単結晶Ｓｉ層には何ら変化はなかった。

【０１５２】透過電子顕微鏡による断面観察の結果、Ｓｉ層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。実施例１と同様にして上述の工程を繰り返し、高品質な半導体層を有する基板複数個を得た。

【０１５３】（実施例７）６２５μｍの厚みを持った比抵抗０．０１Ω・ｃｍのＰ型あるいはＮ型の６インチ径の第１の（１００）単結晶Ｓｉ基板を、ＨＦ溶液中において陽極化成を行った。

【０１５４】陽極化成条件は以下のとおりであった。

【０１５５】電流密度：５（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 1 : 1$

時間：１２（分）

多孔質Ｓｉの厚み：１０（μｍ）

Ｐｏｒｏｓｉｔｙ：１５（％）

この基板を酸素雰囲気中４００℃で１時間酸化した。この酸化により多孔質Ｓｉの孔の内壁は熱酸化膜で覆われた。多孔質Ｓｉ上にＣＶＤ（ＣｈｅｍｉｃａｌＶａｐｏｒ　Ｄｅｐｏｓｉｔｉｏｎ）法により単結晶Ｓｉを１μｍエピタキシャル成長した。成長条件は以下の通りである。

【０１５６】ソースガス：SiH_2Cl_2/H_2

ガス流量：０．５／１８０　ｌ／ｍｉｎ

ガス圧力：８０Ｔｏｒｒ

温度：９５０℃

成長速度：０．３μｍ／ｍｉｎ

さらに、このエピタキシャルＳｉ層表面に熱酸化により１００ｎｍのＳｉO_2層を形成した。

【０１５７】該ＳｉO_2層表面と別に用意した５００ｎｍのＳｉO_2層を形成したＳｉ基板の表面とを重ね合わせ、接触させた後、９００℃－２時間の熱処理をし、貼り合わせをおこなった。

【０１５８】実施例１の手法を用いて、貼り合わせたウェハの面に対して垂直方向に十分な引っ張り力を加えたところ多孔質Ｓｉ層が破壊しウェハは二分割され、多孔質Ｓｉが表出した。

【０１５９】その後、多孔質Ｓｉ層を単結晶Ｓｉをストッパーとして選択研磨した。多孔質Ｓｉ選択研磨され、完全に除去された。

【０１６０】すなわち、Ｓｉ酸化膜上に１μｍの厚みを持った単結晶Ｓｉ層が形成できた。多孔質Ｓｉの選択エッチングによっても単結晶Ｓｉ層には何ら変化はなかった。

【０１６１】透過電子顕微鏡による断面観察の結果、Ｓｉ層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。実施例１と同様にして上述の工程を繰り返し、高品質な半導体層を有

する基板複数個を得た。

【０１６２】（実施例８）６２５μｍの厚みを持った比抵抗０．０１Ω・ｃｍのＰ型あるいはＮ型の６インチ径の第１の（１００）単結晶Ｓｉ基板を、ＨＦ溶液中において陽極化成を行った。

【０１６３】陽極化成条件は以下のとおりであった。

【０１６４】電流密度：５（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 1 : 1$

時間：１２（分）

多孔質Ｓｉの厚み：１０（μｍ）

Ｐｏｒｏｓｉｔｙ：１５（％）

この基板を酸素雰囲気中４００℃で１時間酸化した。この酸化により多孔質Ｓｉの孔の内壁は熱酸化膜で覆われた。多孔質Ｓｉ上にＣＶＤ（ＣｈｅｍｉｃａｌＶａｐｏｒ　Ｄｅｐｏｓｉｔｉｏｎ）法により単結晶Ｓｉを１μｍエピタキシャル成長した。成長条件は以下の通りである。

【０１６５】ソースガス：SiH_2Cl_2 / H_2

ガス流量：０．５／１８０　ｌ／ｍｉｎ

ガス圧力：８０Ｔｏｒｒ

温度：９５０℃

成長速度：０．３μｍ／ｍｉｎ

さらに、このエピタキシャルＳｉ層表面に熱酸化により１００ｎｍのSiO_2層を形成した。

【０１６６】該SiO_2層表面と別に用意した５００ｎｍのSiO_2層を形成したＳｉ基板の表面とを重ね合わせ、接触させた後、９００℃－２時間の熱処理をし、貼り合わせをおこなった。次いで貼り合わせた基板を超音波振動子を配した層の中に入れ、超音波エネルギーを印加したところ多孔質Ｓｉ層が破壊しウェハは二分割され、多孔質Ｓｉが表出した。

【０１６７】その後、多孔質Ｓｉ層を４９％弗酸と３０％過酸化水素水との混合液（１：５）で撹はんしながら選択エッチングする。単結晶Ｓｉはエッチングされずに残り、単結晶Ｓｉをエッチ・ストップの材料として、多孔質Ｓｉは選択エッチングされ完全に除去された。

【０１６８】非多孔質Ｓｉ単結晶の該エッチング液にたいするエッチング速度は、極めて低く、多孔質層のエッチング速度との選択比は十の五乗以上にも達し、非多孔質層におけるエッチング量（数十オングストローム程度）は実用上無視できる膜厚減少である。

【０１６９】すなわち、Ｓｉ酸化膜上に１μｍの厚みを持った単結晶Ｓｉ層が形成できた。多孔質Ｓｉの選択エッチングによっても単結晶Ｓｉ層には何ら変化はなかった。

【０１７０】透過電子顕微鏡による断面観察の結果、Ｓｉ層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【０１７１】第１のＳｉ単結晶基板は残留多孔質Ｓｉを除去して、再度第１のＳｉ単結晶基板として使用した。

【０１７２】（実施例９）５２５μｍの厚みを持った比抵抗０．０１Ω・ｃｍのＰ型あるいはＮ型の４インチ径の第１の（１００）単結晶Ｓｉ基板を、ＨＦ溶液中において陽極化成を行った。

【０１７３】陽極化成条件は以下のとおりであった。

【０１７４】電流密度：７（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 1 : 1$

時間：１２（分）

多孔質Ｓｉの厚み：１０（μｍ）

Ｐｏｒｏｓｉｔｙ：１５（％）

この基板を酸素雰囲気中４００℃で２時間酸化した。この酸化により多孔質Ｓｉの孔の内壁は熱酸化膜で覆われた。多孔質Ｓｉ上にＭＢＥ（Ｍｏｌｅｃｕｌａｒ　Ｂｅａｍ　Ｅｐｉｔａｘｙ）法により単結晶Ｓｉを０．５μｍエピタキシャル成長した。成長条件は以下の通りである。

【０１７５】温度：７００℃

圧力：1×10^{-9}Ｔｏｒｒ

成長速度：０．１ｎｍ／ｓｅｃ

温度：９５０℃

成長速度：０．３μｍ／ｍｉｎ

さらに、このエピタキシャルＳｉ層表面に熱酸化により１００ｎｍのSiO_2層を形成した。

【０１７６】該SiO_2層表面と別に用意した溶融石英基板の表面とを重ね合わせ、接触させた後、４００℃－２時間の熱処理をし、貼り合わせをおこなった。

【０１７７】ウェハ端面に多孔質層を表出させ、多孔質Ｓｉをある程度エッチングし、そこへ剃刀の刃のように鋭利な板を挿入したところ多孔質Ｓｉ層が破壊しウェハは二分割され、多孔質Ｓｉが表出した。

【０１７８】その後、多孔質Ｓｉ層をバッファード弗酸と３０％過酸化水素水との混合液（１：５）で撹はんしながら選択エッチングする。単結晶Ｓｉはエッチングされずに残り、単結晶Ｓｉをエッチ・ストップの材料として、多孔質Ｓｉは選択エッチングされ完全に除去された。

【０１７９】非多孔質Ｓｉ単結晶の該エッチング液にたいするエッチング速度は、極めて低く、多孔質層のエッチング速度との選択比は十の五乗以上にも達し、非多孔質層におけるエッチング量（数十オングストローム程度）は実用上無視できる膜厚減少である。

【０１８０】すなわち、溶融石英基板上に０．５μｍの厚みを持った単結晶Ｓｉ層が形成できた。多孔質Ｓｉの選択エッチングによっても単結晶Ｓｉ層には何ら変化はなかった。

【０１８１】透過電子顕微鏡による断面観察の結果、Ｓｉ層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【０１８２】エピタキシャルＳｉ層表面に酸化膜を形成しなくても同様の結果が得られた。

【０１８３】第１のＳｉ単結晶基板は残留多孔質Ｓｉを除去して、表面研磨を行い鏡面状にした後、再度第１のＳｉ単結晶基板として使用した。

【０１８４】（実施例１０）６２５μｍの厚みを持った比抵抗０．０１Ω・ｃｍのｐ型あるいはＮ型の両面研磨の６インチ径の第１の（１００）単結晶Ｓｉ基板を、ＨＦ溶液中において両面に対して陽極化成を行った。

【０１８５】陽極化成条件は以下のとおりであった。

【０１８６】電流密度：５（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 1 : 1$

時間：１２×２（分）

多孔質Ｓｉの厚み：各１０（μｍ）

Ｐｏｒｏｓｉｔｙ：１５（％）

この基板を酸素雰囲気中４００℃で１時間酸化した。この酸化により多孔質Ｓｉの孔の内壁は熱酸化膜で覆われた。両面に形成した多孔質Ｓｉ上にＣＶＤ（Ｃｈｅｍｉｃａｌ　Ｖａｐｏｒ　Ｄｅｐｏｓｉｔｉｏｎ）法により単結晶Ｓｉを１μｍエピタキシャル成長した。成長条件は以下の通りである。

【０１８７】ソースガス：SiH_2Cl_2/H_2

ガス流量：０．５／１８０　ｌ／ｍｉｎ

ガス圧力：８０Ｔｏｒｒ

温度：９５０℃

成長速度：０．３μｍ／ｍｉｎ

さらに、このエピタキシャルＳｉ層表面に熱酸化により１００ｎｍのSiO_2層を形成した。

【０１８８】該SiO_2層表面と別に用意した５００ｎｍのSiO_2層を形成した２枚のＳｉ基板の表面とをそれぞれ重ね合わせ、接触させた後、６００℃－２時間の熱処理をし、貼り合わせをおこなった。

【０１８９】ウェハ端面に多孔質層を表出させ、多孔層Ｓｉに水等の液体をしみ込ませた後、貼り合わせウェハ全体を加熱あるいは冷却したところ、液体の膨張等により多孔質Ｓｉ層が破壊しウェハは二分割され、多孔質Ｓｉが表出した。

【０１９０】その後、多孔質Ｓｉ層を４９％弗酸と３０％過酸化水素水との混合液（１：５）で撹はんしながら選択エッチングする。単結晶Ｓｉはエッチングされずに残り、単結晶Ｓｉをエッチ・ストップの材料として、多孔質Ｓｉは選択エッチングされ完全に除去された。

【０１９１】非多孔質Ｓｉ単結晶の該エッチング液に対するエッチング速度は、極めて低く、多孔質層のエッチング速度との選択比は十の五乗以上にも達し、非多孔質層におけるエッチング量（数十オングストローム程度）は実用上無視できる膜厚減少である。

【０１９２】すなわち、Ｓｉ酸化膜上に１μｍの厚みを持った単結晶Ｓｉ層が２枚同時に形成できた。多孔質Ｓｉの選択エッチングによっても単結晶Ｓｉ層には何ら変化はなかった。

【０１９３】透過電子顕微鏡による断面観察の結果、Ｓｉ層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【０１９４】エピタキシャルＳｉ層表面に酸化膜を形成しなくても同様の結果が得られた。

【０１９５】第１のＳｉ単結晶基板は残留多孔質Ｓｉを除去して、表面を水素処理して平坦化した後、再度第１のＳｉ単結晶基板として使用した。

【０１９６】（実施例１１）６２５μｍの厚みを持った比抵抗０．０１Ω・ｃｍのｐ型あるいはＮ型の５インチ径の第１の（１００）単結晶Ｓｉ基板を、ＨＦ溶液中において陽極化成を行った。

【０１９７】陽極化成条件は以下のとおりであった。

【０１９８】電流密度：７（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 1 : 1$

時間：４（分）

多孔質Ｓｉの厚み：３（μｍ）

Ｐｏｒｏｓｉｔｙ：１５（％）

さらに

電流密度：３０（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 3 : 2$

時間：３（分）

多孔質Ｓｉの厚み：１０（μｍ）

Ｐｏｒｏｓｉｔｙ：４５（％）

この基板を酸素雰囲気中４００℃で１時間酸化した。この酸化により多孔質Ｓｉの孔の内壁は熱酸化膜で覆われた。多孔質Ｓｉ上にＣＶＤ法により単結晶Ｓｉを０．３μｍエピタキシャル成長した。成長条件は以下の通りである。

【０１９９】ソースガス：SiH_4

キャリヤーガス：H_2

温度：８５０℃

圧力：1×10^{-2}Ｔｏｒｒ

成長速度：３．３ｎｍ／ｓｅｃ

さらに、このエピタキシャルＳｉ層表面に熱酸化により１００ｎｍのSiO_2層を形成した。

【０２００】該SiO_2層表面と別に用意した５００ｎｍのSiO_2層を形成したＳｉ基板の表面とを重ね合わせ、接触させた後、７００℃－２時間の熱処理をし、貼り合わせをおこなった。

【０２０１】第１（あるいは第２）の基板に対して第２（あるいは第１）の基板に水平方向に力を加えたところ多孔質Ｓｉ層は剪断応力に耐えきれず破壊しウェハは二分割され、多孔質Ｓｉが表出した。

【０２０２】その後、多孔質Ｓｉ層を$HF/HNO_3/CH_3COOH$系のエッチング液で選択エッチングす

る。多孔質Ｓｉは選択エッチングされ完全に除去された。

【０２０３】非多孔質Ｓｉ単結晶の該エッチング液にたいするエッチング速度は、極めて低く、非多孔質層におけるエッチング量は実用上無視できる膜厚減少である。

【０２０４】すなわち、Ｓｉ酸化膜上に１μｍの厚みを持った単結晶Ｓｉ層が形成できた。多孔質Ｓｉの選択エッチングによっても単結晶Ｓｉ層には何ら変化はなかった。

【０２０５】透過電子顕微鏡による断面観察の結果、Ｓｉ層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【０２０６】エピタキシャルＳｉ層表面に酸化膜を形成しなくても同様の結果が得られた。

【０２０７】第１のＳｉ単結晶基板は残留多孔質Ｓｉを除去して、再度第１のＳｉ単結晶基板として使用した。

【０２０８】（実施例１２）６２５μｍの厚みを持った比抵抗０．０１Ω・ｃｍのＰ型あるいはＮ型の５インチ径の第１の（１００）単結晶Ｓｉ基板を、ＨＦ溶液中において陽極化成を行った。

【０２０９】陽極化成条件は以下のとおりであった。

【０２１０】電流密度：７（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 1 : 1$

時間：４（分）

多孔質Ｓｉの厚み：３（μｍ）

Ｐｏｒｏｓｉｔｙ：１５（％）

さらに

電流密度：３０（$mA \cdot cm^{-2}$）

陽極化成溶液：$HF : H_2O : C_2H_5OH = 1 : 3 : 2$

時間：３（分）

多孔質Ｓｉの厚み：１０（μｍ）

Ｐｏｒｏｓｉｔｙ：４５（％）

この基板を酸素雰囲気中４００℃で１時間酸化した。この酸化により多孔質Ｓｉの孔の内壁は熱酸化膜で覆われた。多孔質Ｓｉ上にＣＶＤ法により単結晶Ｓｉを０．３μｍエピタキシャル成長した。成長条件は以下の通りである。

【０２１１】ソースガス：SiH_4

キャリヤーガス：H_2

温度：８５０℃

圧力：1×10^{-2}Ｔｏｒｒ

成長速度：３．３ｎｍ／ｓｅｃ

さらに、このエピタキシャルＳｉ層表面に熱酸化により１００ｎｍのSiO_2層を形成した。

【０２１２】該SiO_2層表面と別に用意した５００ｎｍのSiO_2層を形成したＳｉ基板の表面とを重ね合わせ、接触させた後、７００℃－２時間の熱処理をし、貼り合わせをおこなった。

【０２１３】ウェハ端面に多孔質層を表出させ、多孔質Ｓｉの選択エッチング液により端面から多孔質Ｓｉ層をエッチングしたところウェハは二分割された。

【０２１４】その後、多孔質Ｓｉ層を$HF／HNO_3／CH_3COOH$系のエッチング液で選択エッチングする。多孔質Ｓｉは選択エッチングされ完全に除去された。

【０２１５】非多孔質Ｓｉ単結晶の該エッチング液にたいするエッチング速度は、極めて低く、非多孔質層におけるエッチング量は実用上無視できる膜厚減少である。

【０２１６】すなわち、Ｓｉ酸化膜上に１μｍの厚みを持った単結晶Ｓｉ層が形成できた。多孔質Ｓｉの選択エッチングによっても単結晶Ｓｉ層には何ら変化はなかった。

【０２１７】透過電子顕微鏡による断面観察の結果、Ｓｉ層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【０２１８】エピタキシャルＳｉ層表面に酸化膜を形成しなくても同様の結果が得られた。

【０２１９】第１のＳｉ単結晶基板は残留多孔質Ｓｉを除去して、再度第１のＳｉ単結晶基板として使用した。

【０２２０】

【発明の効果】以上説明したように、本発明によれば、貼り合わせて構成された基体を多孔質層で分離し、非多孔質単結晶半導体層が配された第２の基体上の多孔質層を除去することにより、高品質な非多孔質単結晶半導体層が配された半導体基体を形成できる。

【０２２１】これに加えて、貼り合わせて構成された基体を多孔質層で分離し、第１の基体を構成する多孔質層を除去することにより、多孔質層を除去した第１の基体を半導体基体作製に再利用することができるため、半導体基体の生産性の向上、低コスト化が更に図れる。

【０２２２】また、本発明によれば、透明基板（光透過性基板）をはじめとする基板上に結晶性が単結晶ウェハ一並に優れたＳｉ等の単結晶層あるいは化合物半導体単結晶層を得るうえで、生産性、均一性、制御性、コストの面において卓越した半導体基板の作製方法を提案することができる。

【０２２３】また、本発明によれば、ＳＯＩ構造の大規模集積回路を作製する際にも、高価なＳＯＳや、ＳＩＭＯＸの代替足り得る半導体基板の作製方法を提案することができる。

【０２２４】また、本発明によれば、多孔質層を介して基体を２つ以上に分離することができ、分離後の一方の基体は、残留多孔質を除去した後、半導体基板として使用可能であり、他方の基体は、残留多孔質を除去した後、再度、半導体基板の作製に利用することができる。

【０２２５】また、本発明によれば、基体の両面に多孔質層および非多孔質単結晶層を形成し、該単結晶層を挟むように２枚の別の基体を貼り合わせた後、前記多孔質

層で基体を分離することにより同時に２枚の半導体基板を作製することができる。

【０２２６】すなわち、本発明によれば、経済性に優れて、大面積に渡り均一平坦な、極めて優れた結晶性を有する単結晶基板を用いて、表面に形成された半導体層あるいは化合物半導体活性層を残して、その片面から該活性層までを取り去り、絶縁物上に欠陥の著しく少ない単結晶層あるいは化合物半導体結晶層を得る半導体基板の作製方法を提供することができる。

【０２２７】また、透明基板（光透過性基板）上に結晶性が単結晶ウェハー並に優れたＳｉあるいは化合物半導体単結晶層を得るうえで、生産性、均一性、制御性、コストの面において卓越した半導体基板の作製方法を得ることができる。

【０２２８】また、ＳＯＩ構造の大規模集積回路を作製する際にも、高価なＳＯＳや、ＳＩＭＯＸの代替足り得る半導体基板の作製方法を得ることができる。

【図面の簡単な説明】

【図１】本発明の方法の１例を説明するための模式的断面図である。

【図２】本発明の方法の１例を説明するための模式的断面図である。

【図３】本発明の方法の１例を説明するための模式的断面図である。

【図４】本発明の方法の１例を説明するための模式的断面図である。

【図５】本発明の方法の１例を説明するための模式的断面図である。

【符号の説明】

１１　Ｓｉ単結晶基板

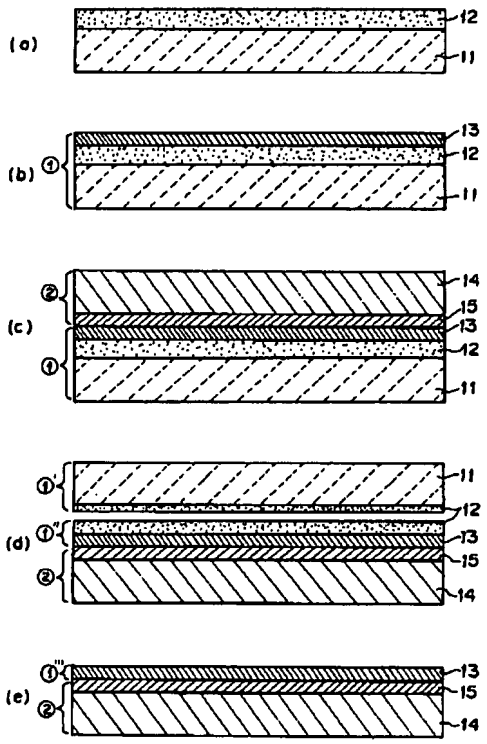
１２　多孔質Ｓｉ層

１３　非多孔質単結晶Ｓｉ層

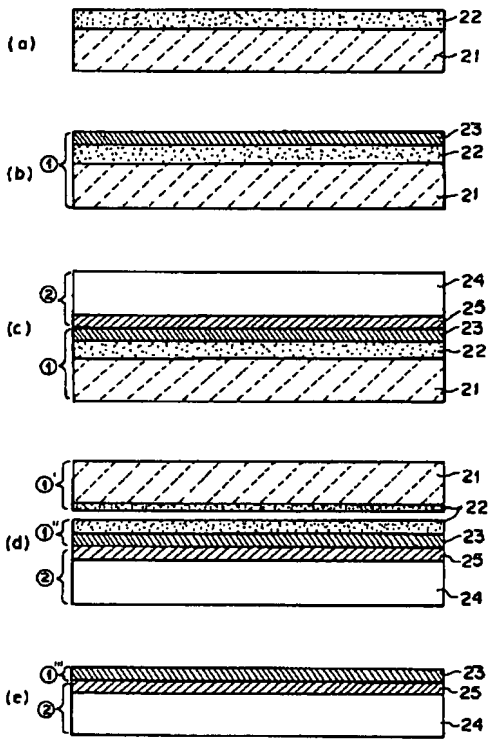
１４　Ｓｉ支持基板

１５　絶縁層

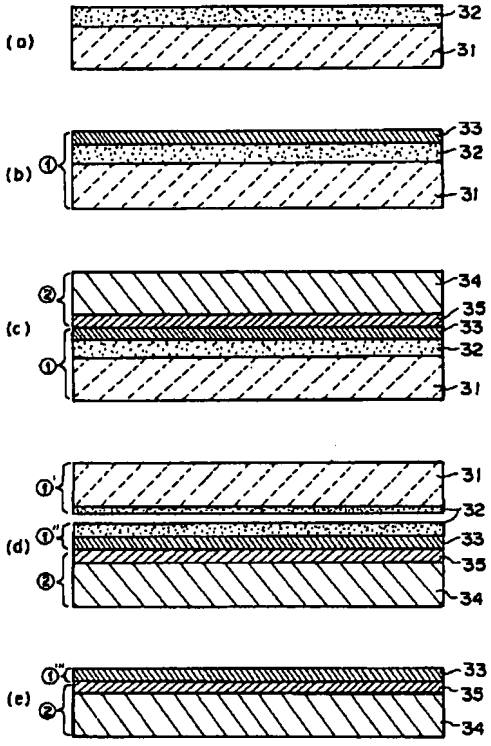
【図１】



【図２】



【図３】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(b)
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(c)
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(d)
①'
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②
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(e)
①'''
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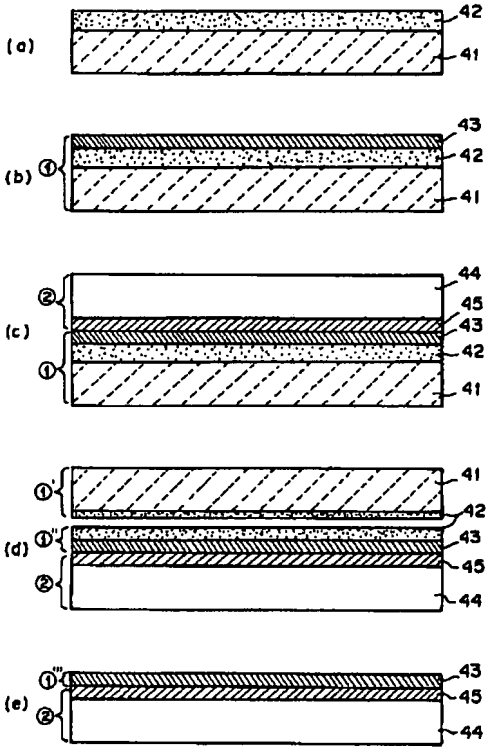
②
35
34

【図４】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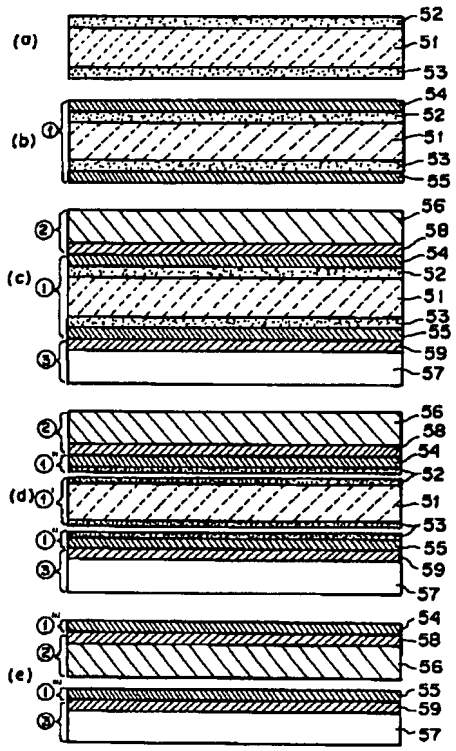
【図５】



フロントページの続き

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23/12				
23/15				
			Ｈ０１Ｌ　23/14	Ｃ